SGM42560/SGM42561/SGM42562
18V, 2.5A Three-Phase Integrated FET Motor Drivers

GENERAL DESCRIPTION

The SGM42560/1/2 family is a triple half-bridge driver, which is designed to drive three-phase brushless DC motors. The device integrates three current sense amplifiers (CSA) for sensing the three phase currents of BLDC motor.

For SGM42560, the ENx and PWMx control inputs are provided for each half-bridge. For SGM42561, the HSx (high-side control inputs) and LSx (low-side control inputs) are provided for each half-bridge, while SGM42562 has the hall-signal (Hx) interface. The required high-side gate drive voltages are generated by an internal charge pump.

The device has multiple protection functions, including under-voltage lockout (UVLO), over-current protection (OCP) and thermal shutdown (TSD). The nFAULT pin is used to indicate the fault problems.

The SGM42560/1/2 are available in a Green TQFN-3×4-24L package.

FEATURES

- **Operating Supply Voltage: 3V to 18V**
- **High Output Current Capability**
  - **2.5A Continuous Current**
  - **5A Peak Current**
- **On-Resistance: 170mΩ (HS + LS) at +25℃**
- **Control Inputs**
  - **SGM42560: ENx and PWMx**
  - **SGM42561: HSx and LSx**
  - **SGM42562: Hall-Signal (Hx)**
- **Integrated Low-side Current Sensing**
- **Built-in LDO Regulator: 3.3V, 50mA**
- **Supports 100% PWM Duty Cycle Driving**
- **Automatic Synchronous Rectification**
- **Integrated Protection Features**
  - **Under-Voltage Lockout (UVLO)**
  - **Over-Current Protection (OCP) with Adjustable Threshold**
  - **Thermal Shutdown (TSD)**
- **Available in a Green TQFN-3×4-24L Package**

APPLICATIONS

Three-Phase BLDC Motor Drivers

TYPICAL APPLICATION

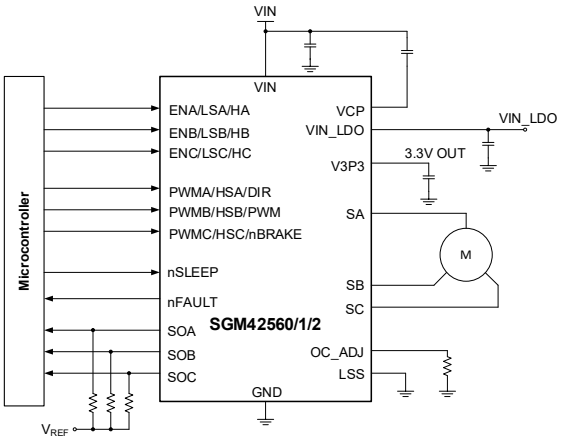


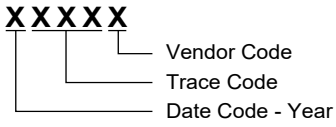
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42560	TQFN-3×4-24L	-40℃ to +125℃	SGM42560XTRR24G/TR	SGM 42560TRR XXXXX	Tape and Reel, 4000
SGM42561	TQFN-3×4-24L	-40℃ to +125℃	SGM42561XTRR24G/TR	SGM 42561TRR XXXXX	Tape and Reel, 4000
SGM42562	TQFN-3×4-24L	-40℃ to +125℃	SGM42562XTRR24G/TR	SGM 42562TRR XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN}, V_{IN_LDO} ..... -0.3V to 20V
V_{Sx} ..... -0.3V to V_{IN} + 0.3V
V_{CP} ..... -0.3V to V_{IN} + 5V
GND to LSS ..... -0.3V to 0.3V
Voltage at All Other Pins ..... -0.3V to 5V
Package Thermal Resistance
TQFN-3×4-24L, θ_{JA} ..... 37℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN}, V_{IN_LDO} ..... 3V to 18V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

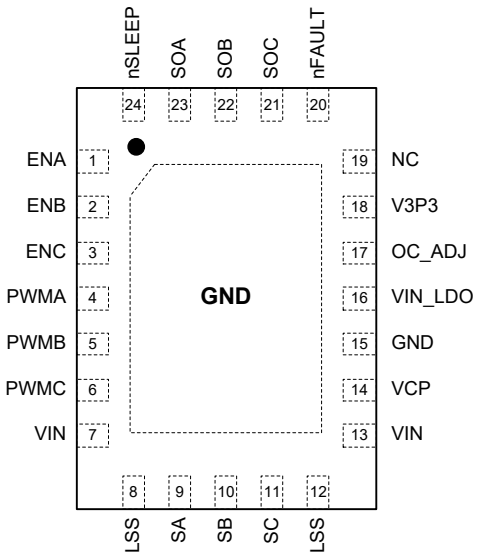
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

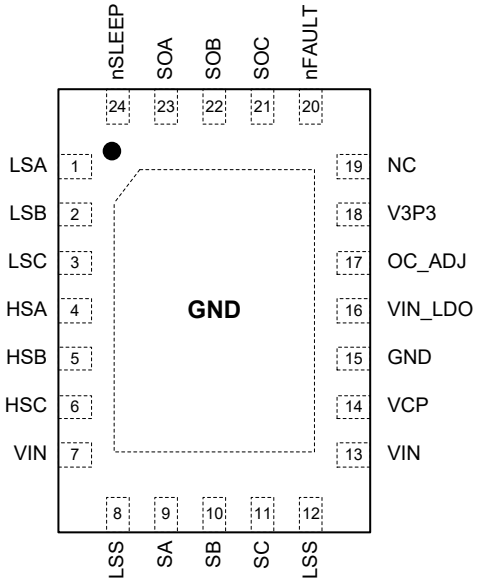
PIN CONFIGURATION

SGM42560 (TOP VIEW)



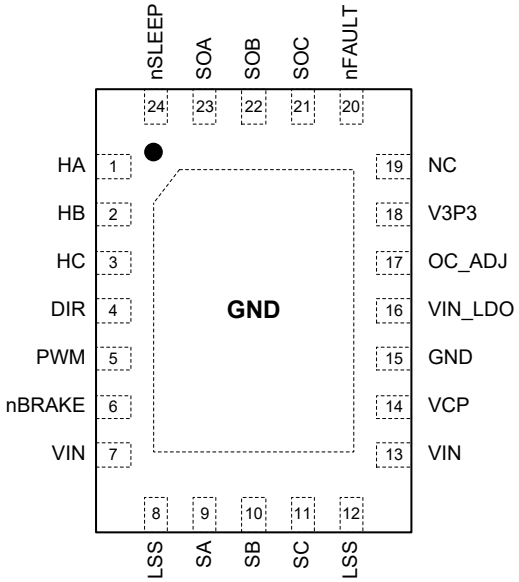
TQFN-3×4-24L

SGM42561 (TOP VIEW)



TQFN-3×4-24L

SGM42562 (TOP VIEW)



TQFN-3×4-24L

PIN DESCRIPTION

PIN	NAME			FUNCTION
	SGM42560	SGM42561	SGM42562	
1	ENA	-	-	Phase A Enable Input.
	-	LSA	-	Phase A Low-side FET Enable Input.
	-	-	HA	Phase A Hall-Signal Input.
2	ENB	-	-	Phase B Enable Input.
	-	LSB	-	Phase B Low-side FET Enable Input.
	-	-	HB	Phase B Hall-Signal Input.
3	ENC	-	-	Phase C Enable Input.
	-	LSC	-	Phase C Low-side FET Enable Input.
	-	-	HC	Phase C Hall-Signal Input.
4	PWMA	-	-	Phase A PWM Input.
	-	HSA	-	Phase A High-side FET Enable Input.
	-	-	DIR	Direction Input Pin.
5	PWMB	-	-	Phase B PWM Input.
	-	HSB	-	Phase B High-side FET Enable Input.
	-	-	PWM	External PWM Control for Speed/Torque.
6	PWMC	-	-	Phase C PWM Input.
	-	HSC	-	Phase C High-side FET Enable Input.
	-	-	nBRAKE	Active-Low Logic Input for Braking Function.
7, 13	VIN			Supply Voltage.
8, 12	LSS			Low-side Source Connection. Directly connected to GND.
9	SA			Output of Phase A.
10	SB			Output of Phase B.
11	SC			Output of Phase C.
14	VCP			Charge Pump Output. Decouple with a 1μF ceramic capacitor to VIN pin.
15	GND			Ground.
16	VIN_LDO			V3P3 LDO Supply Voltage.
17	OC_ADJ			Adjustable Over-Current Threshold.
18	V3P3			3.3V Voltage Regulator Output. A 0.47μF ceramic capacitor is used between V3P3 and GND pins.
19	NC			No Connection.
20	nFAULT			Fault Even Indication Pin. Go logic low when a fault occurs. Open-drain output.
21	SOC			Phase C Current Sense Output.
22	SOB			Phase B Current Sense Output.
23	SOA			Phase A Current Sense Output.
24	nSLEEP			Sleep Mode Input. Active-low sleep mode logic input with weak internal pull-down. Apply high to enable device, and low to enter into the low power sleep mode.
Exposed Pad	GND			Ground.

ELECTRICAL CHARACTERISTICS

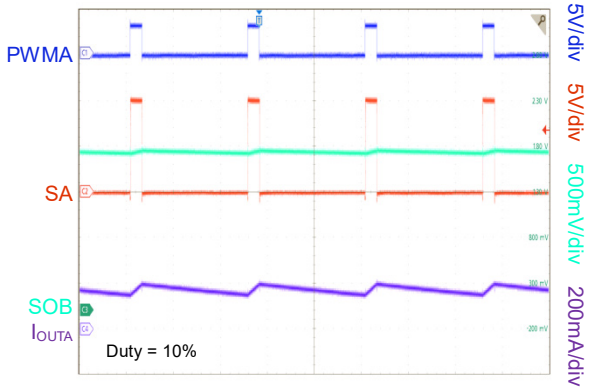
(T_J = +25℃, V_{IN} = 10V, LSS = GND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Input Supply Voltage	V_{IN}, V_{IN_LDO}			3		18	V
Quiescent Current	I_Q	nSLEEP = high, ENx = low			2.8	3.6	mA
	I_{nSLEEP}	nSLEEP = low			45	60	μA
Control Logic							
Input Low Threshold	V_{IL}					0.4	V
Input High Threshold	V_{IH}			1.5			V
Logic Input Current	I_{INH}	V_{IN} = 5V		-20		20	μA
	I_{INL}	V_{IN} = 0V		-20		20	μA
Power-Up Delay	t_{PUD}	At V_{IN} rising or nSLEEP rising			0.8		ms
Internal Pull-Down Resistance	R_{PD}	All logic inputs			500		kΩ
nFAULT Pull-Down R_{ON}	R_{ON_nFAULT}				5		Ω
V3P3 Regulator							
V3P3 Pin Voltage	V_{V3P3}	I_{OUT} = 0mA to 50mA		3.30	3.47	3.65	V
Protection Circuits							
UVLO Threshold	V_{UVLO}	V_{IN} rising		2.64	2.8	2.95	V
UVLO Hysteresis	ΔV_{UVLO}				200		mV
OCP Threshold	I_{OCP}	Measure in test mode	R_{OCP} = 0Ω	2.5	3.5	4.5	A
			R_{OCP} = Floating	4.6	6.0	8.0	A
OCP Deglitch Time	t_{OCD}				1		μs
Thermal Shutdown Threshold	T_{TSD}	T_J rising			170		℃
Thermal Shutdown Hysteresis	T_{HYS}				30		℃
Current Sense							
Current Sense Ratio				1/3600	1/4000	1/4400	A/A
Current Sense Output Current		LS FET current = 1A		230	250	270	μA
		LS FET current = -1A		-270	-250	-230	μA
		LS FET current = 100mA		19	25	31	μA
		LS FET current = -100mA		-31	-25	-19	μA
Current Sense Output Voltage Swing		LS FET current = ±0.25A		0.05		3.7	V
Output							
HS FET On-Resistance	R_{DSON}	I_{OUT} = 1A		40	80	125	mΩ
LS FET On-Resistance		I_{OUT} = 1A		40	90	130	
Output Rise Time	t_R	R_{LOAD} = 50Ω			25		ns
Output Fall Time	t_F	R_{LOAD} = 50Ω			25		ns
Dead Time	t_D	R_{LOAD} = 50Ω			40		ns
PWMx to Sx Delay Time Rising	t_{DLY_R}				70		ns
PWMx to Sx Delay Time Falling	t_{DLY_F}				90		ns
Charge Pump							
Charge Pump Output Voltage	V_{CP}				V_{IN} + 3.7		V

TYPICAL PERFORMANCE CHARACTERISTICS

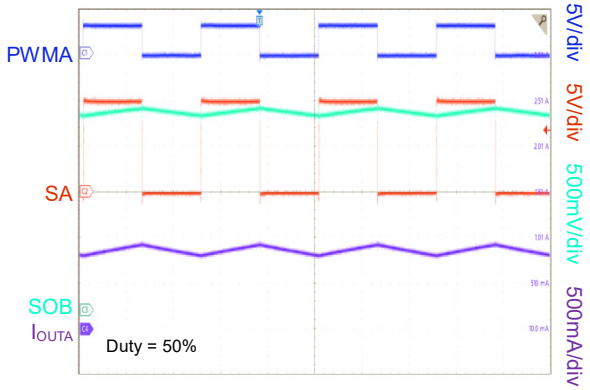
T_J = +25℃, V_{IN} = 10V, V_{REF} = 3.3V, SOB with 5kΩ divide, output with 5Ω + 1mH load, unless otherwise noted.

Steady State



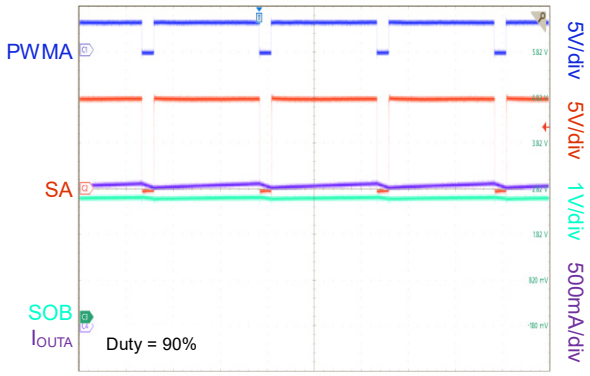
Time (20μs/div)

Steady State



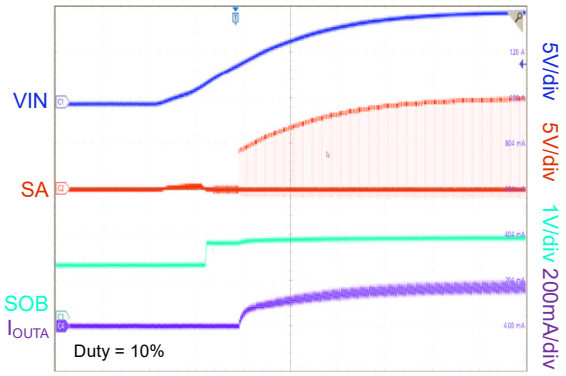
Time (20μs/div)

Steady State



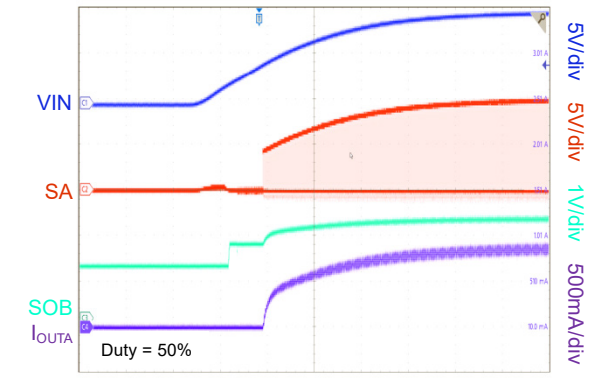
Time (20μs/div)

Power Ramp-Up



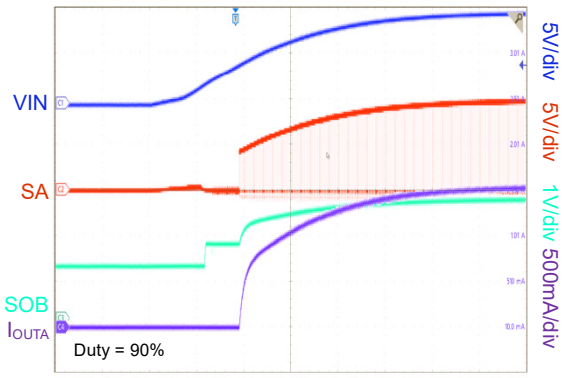
Time (2ms/div)

Power Ramp-Up



Time (2ms/div)

Power Ramp-Up

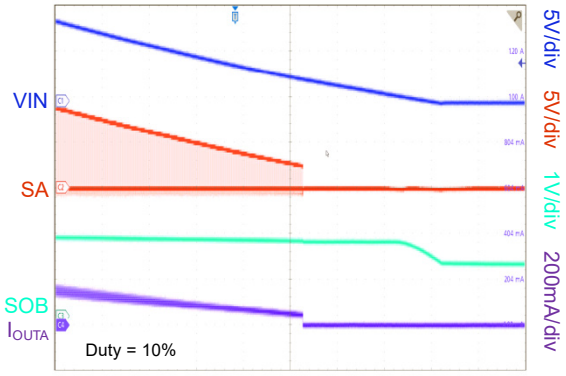


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

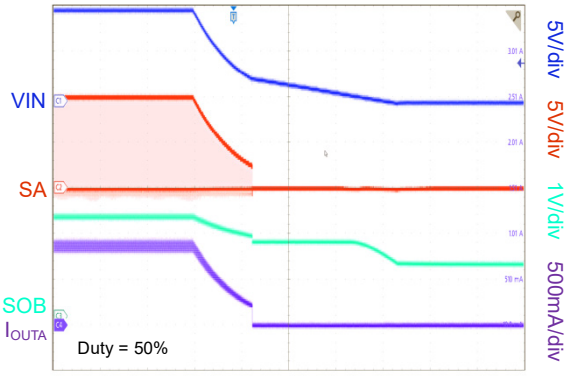
T_J = +25℃, V_{IN} = 10V, V_{REF} = 3.3V, SOB with 5kΩ divide, output with 5Ω + 1mH load, unless otherwise noted.

Power Ramp-Down



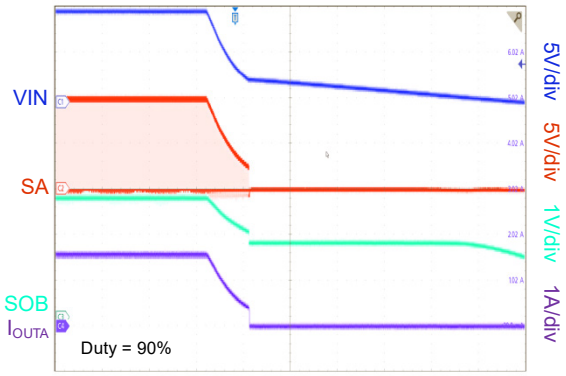
Time (20ms/div)

Power Ramp-Down



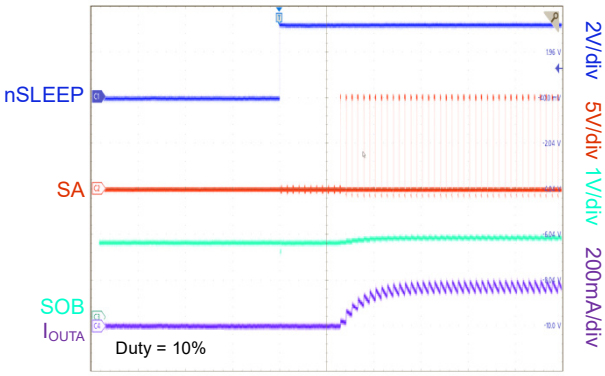
Time (20ms/div)

Power Ramp-Down



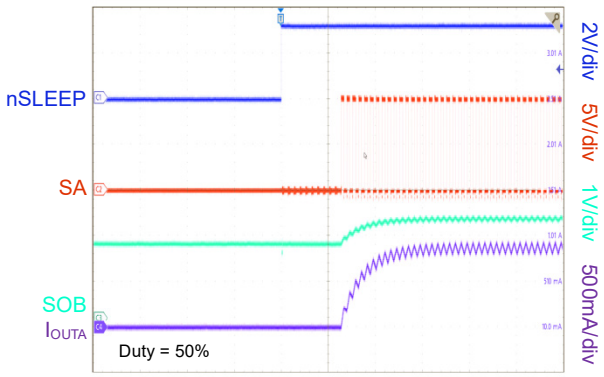
Time (10ms/div)

Sleep Recovery



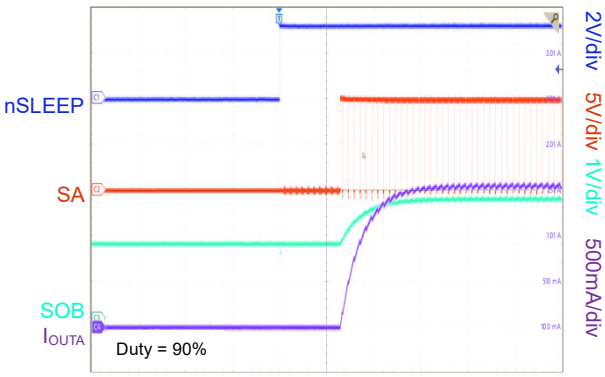
Time (400μs/div)

Sleep Recovery



Time (400μs/div)

Sleep Recovery

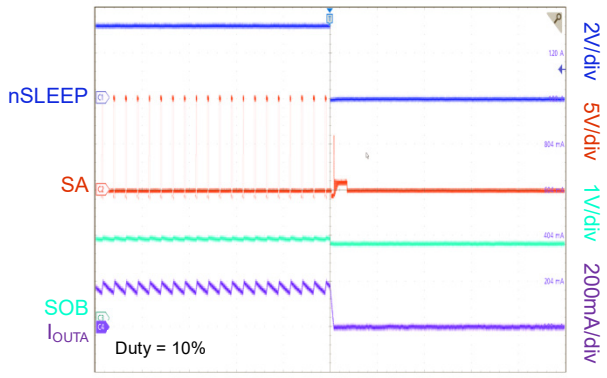


Time (400μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

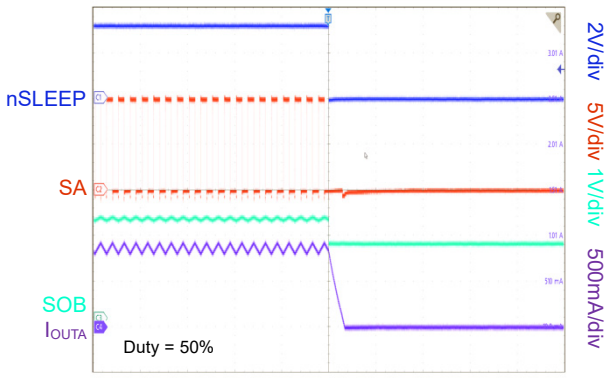
T_J = +25℃, V_{IN} = 10V, V_{REF} = 3.3V, SOB with 5kΩ divide, output with 5Ω + 1mH load, unless otherwise noted.

Sleep Entry



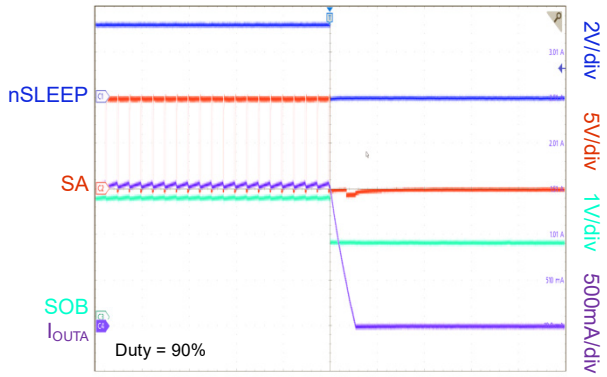
Time (200μs/div)

Sleep Entry



Time (200μs/div)

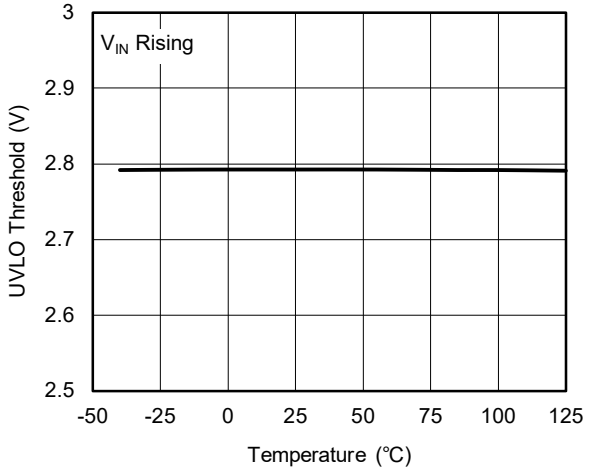
Sleep Entry



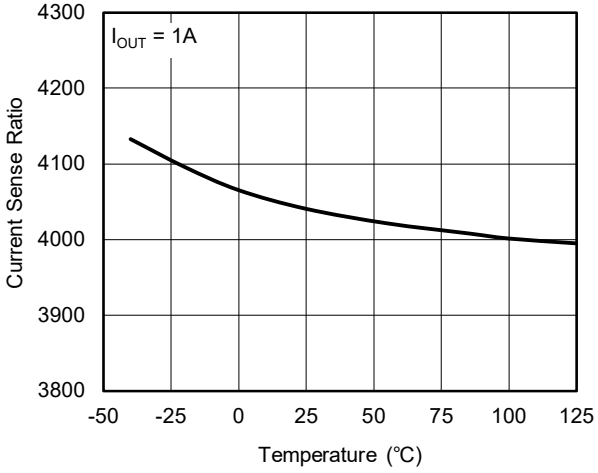
Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

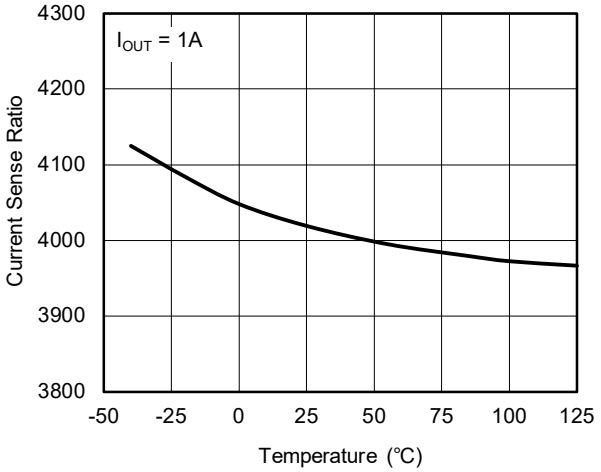
UVLO Threshold vs. Temperature



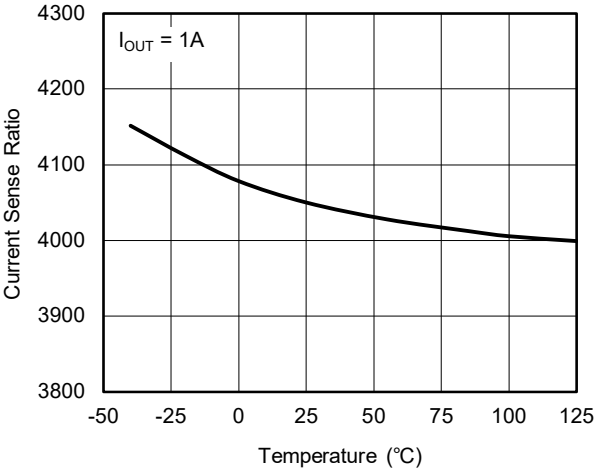
Phase A Current Sense Ratio vs. Temperature



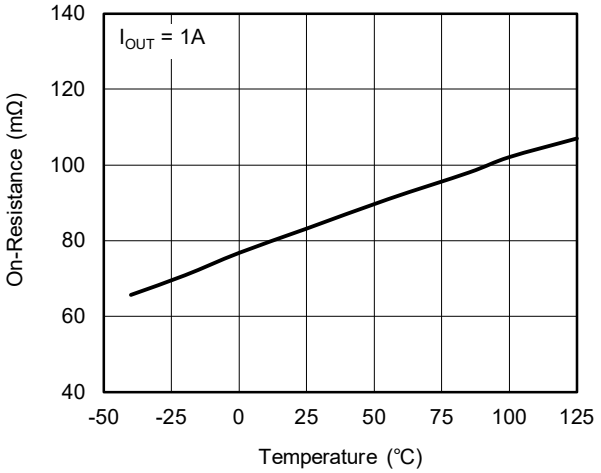
Phase B Current Sense Ratio vs. Temperature



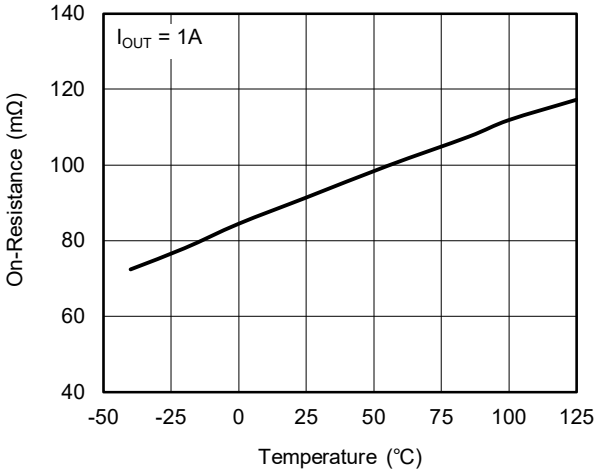
Phase C Current Sense Ratio vs. Temperature



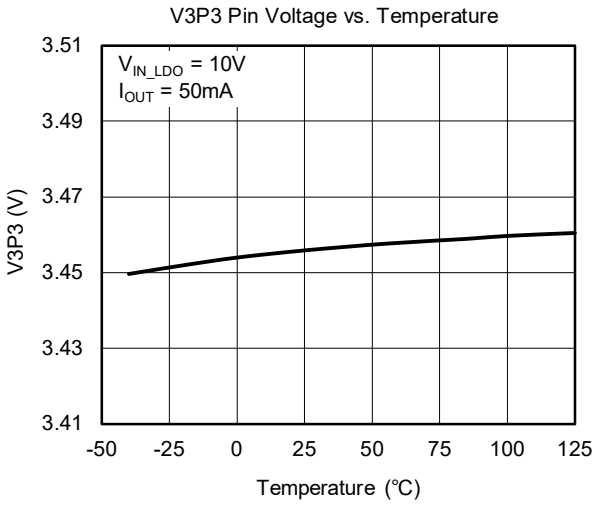
HS FET On-Resistance vs. Temperature



LS FET On-Resistance vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



FUNCTIONAL BLOCK DIAGRAM

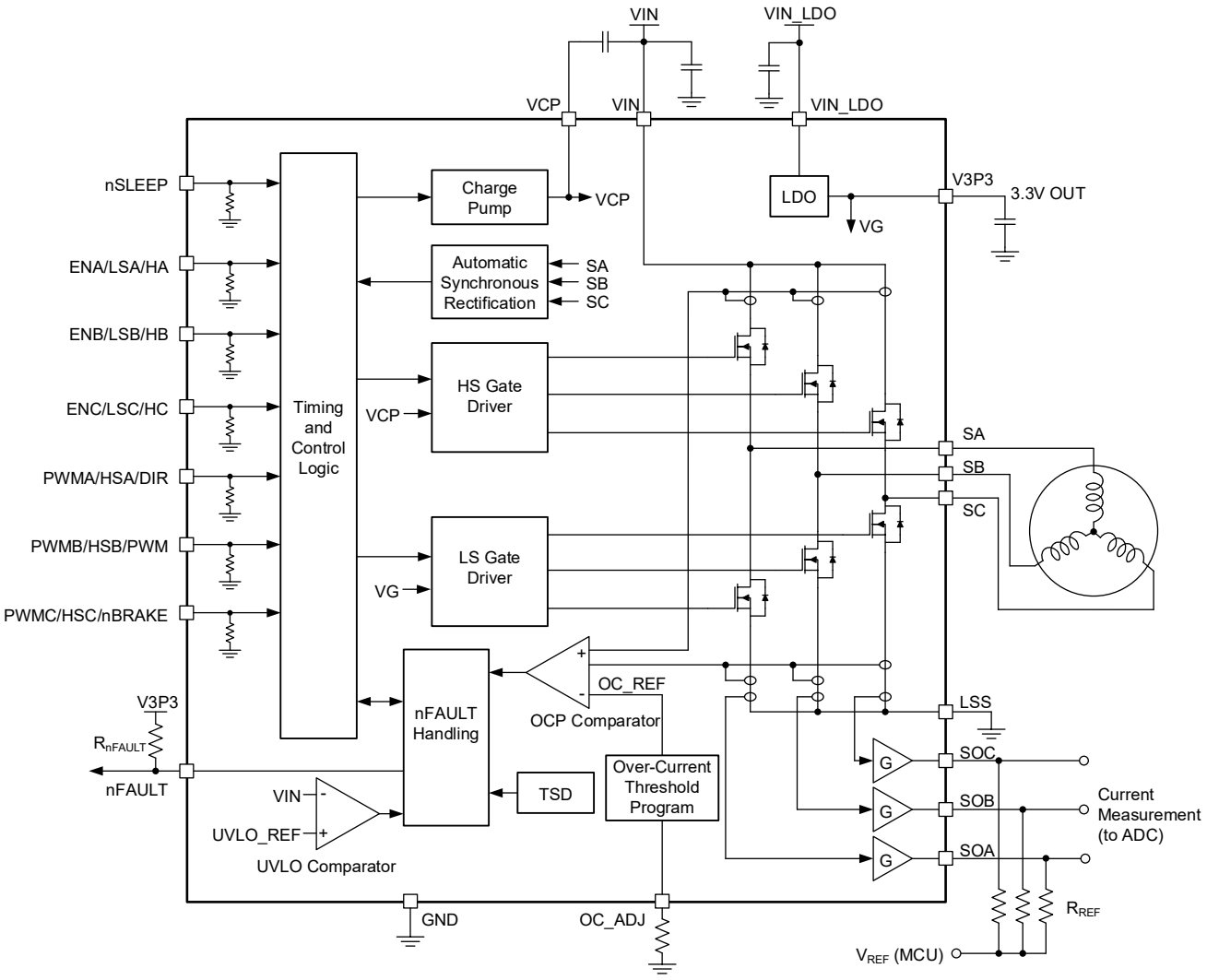


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM42560 family is an integrated 170mΩ (combination of HS and LS FETs on-resistance) driver for three-phase BLDC motor drive applications. The device reduces system component counts, cost and complexity by integrating three half-bridge FETs, current sensing and protection circuits.

Input Logic

The SGM42560 family provides three different control modes to support various commutations and control methods. Please refer to SGM42560 input control logic in Table 1.

Table 1. Truth Table of SGM42560

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	Hi-Z

The SGM42561 has the HSx (high-side control inputs) and LSx (low-side control inputs) provided for each half-bridge. Table 2 shows the logic truth table for SGM42561.

Table 2. Truth Table of SGM42561

HSx	LSx	Sx
L	L	Hi-Z
L	H	GND
H	L	VIN
H	H	Hi-Z

The commutation logic of SGM42562 is controlled by combination logic based on three hall-sensor inputs spacing at 120°. The PWM input controls motor speed, and DIR input controls motor direction. Motor braking can be initiated by the nBRAKE input.

Table 3. Truth Table of SGM42562

PWM	nBRAKE	Mode of Operation
0	1	PWM Chop Mode, the Load Current Decays.
0	0	Brake Mode. All Low-side Gates On.
1	1	Selected Drivers On.
1	0	Brake Mode. All Low-side Gates On.

Table 4. Commutation Table of SGM42562 (nBRAKE = 1)

HA	HB	HC	DIR	SA	SB	SC
1	0	1	1	PWM	Z	L
1	0	0	1	Z	PWM	L
1	1	0	1	L	PWM	Z
0	1	0	1	L	Z	PWM
0	1	1	1	Z	L	PWM
0	0	1	1	PWM	L	Z
1	0	1	0	L	Z	PWM
0	0	1	0	L	PWM	Z
0	1	1	0	Z	PWM	L
0	1	0	0	PWM	Z	L
1	1	0	0	PWM	L	Z
1	0	0	0	Z	L	PWM
0	0	0	x	Z	Z	Z
1	1	1	x	Z	Z	Z

Note that the logic inputs are weak pull-down internally.

DETAILED DESCRIPTION (continued)

nSLEEP Operation

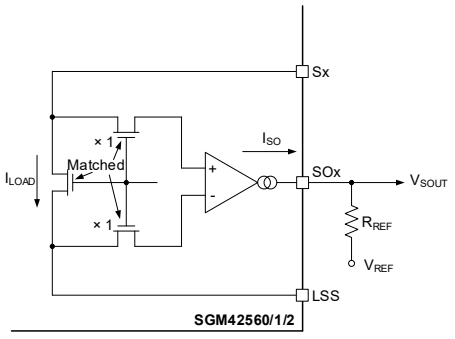
This active-low input is used to minimize power consumption when the device is not in use. Sleep mode disables most of the internal circuitry, including the output FETs and charge pump. Logic high allows normal operation. If the charge pump output capacitor is fully discharged, the device must take about 0.8ms to respond to the inputs. The nSLEEP input is pull-down internally.

Current Sense Amplifiers

The SGM42560 integrates three high performance LS current sense amplifiers for current measurements using built-in current sensing. LS current measurements are commonly used to implement over-current protection, external torque control, or brushless DC commutation with an external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs (LS FETs). Each half-bridge has its own current sensing output (SOx) for sensing the sink or source current flowing through the low-side FET (bi-direction). Connect a resistor (R_{REF}) from SOx to reference voltage will convert the current into a voltage output. Please refer to the Equation 1 for calculation of current and SOx output voltage:

$$V_{SOUT} = V_{REF} + (R_{REF} \times I_{LOAD})/4000 \quad (1)$$

When using an ADC with inputs that are ratio-metric to its supply voltage, the SOx output is connected to the ADC reference power supply and GND through two resistors of the same value. The SOx output will be half of the ADC reference voltage when the current is zero. Please refer to simplified schematic of the current measurement in Figure 3.



$I_{SO} = I_{LOAD}/4000$
$V_{SOUT} = V_{REF} + (I_{SO} \times R_{REF}) = V_{REF} + ((I_{LOAD} \times R_{REF})/4000)$

Figure 3. Current Measurement Circuit Diagram

Automatic Synchronous Rectification

The SGM42560 family has automatic synchronous rectification feature (active demagnetization) which reduces power losses in device by reducing body-diode conduction losses. If both half-bridge power FETs are turned off, then the automatic synchronous rectification applies, the inductor current decays through FETs instead of the body-diodes.

The SGM42560 includes a HS output comparator and a LS output comparator for each half-bridge channel, which detect the respective body-diodes' current flow. The HS output comparator compares the half-bridge output voltage with respect to V_{IN}. The LS output comparator compares the half-bridge output voltage with respect to LSS. When both HS FET and LS FET of a channel are turned off, upon the flow of the recirculation current: if the LS body-diode conducts, the half-bridge output voltage is driven below LSS, and the LS output comparator trips, then the LS FET will be on until the recirculation current reduces to zero. Similarly, if the HS body-diode conducts, the half-bridge output voltage is driven above V_{IN}, and the HS output comparator trips, then the HS FET is turned on until the current flowing through it reduces to zero.

nFAULT Output

The nFAULT is an open-drain output that needs to be pulled up externally. The nFAULT will be pulled low in OC (over-current) or TSD (thermal shutdown) condition.

UVLO Protection

At any time, the V_{IN} power supply falls below the V_{UVLO} threshold (V_{IN} falling threshold), all of the integrated FETs, driver charge pump and digital logic controller are disabled and the internal logic is reset. The device will resume normal operation when power supply goes higher than V_{UVLO} threshold.

Thermal Shutdown (TSD)

All bridges and drivers are shutdown if a junction over-temperature occurs in the device and the nFAULT will be pulled low. Once the temperature goes back to the safe level, the device resumes its operation.

DETAILED DESCRIPTION (continued)

Over-Current Protection

A MOSFET over-current event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the I_{OCP} threshold (refer to Table 5 for setup) for longer than the t_{OCD} deglitch time, all the three half-bridges will be disabled (shutdown), and the nFAULT pin will be driven low. The over-current shutdown is latched until either nSLEEP is reset or VIN is power-cycled.

An over-current may occur due to a short between a switching node and ground or to the VIN supply line, or to the other node of the bridge (a winding short). Figure 4 shows a simplified diagram of the OCP circuit for one output.

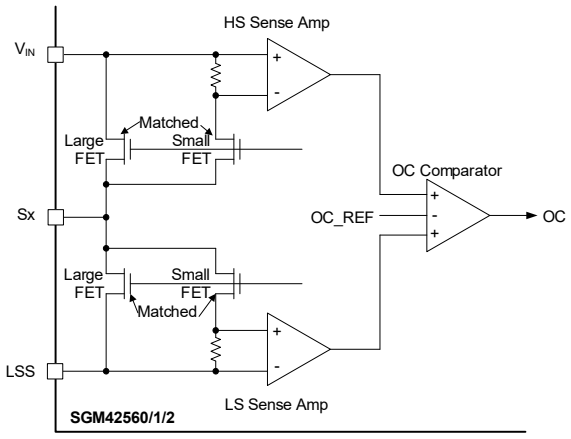


Figure 4. OCP Circuit

Table 5. Over-Current Threshold

OC_ADJ Resistor Value	OCP Threshold (TYP)
0Ω	3.5A
Floating	6.0A

3.3V LDO Output

A 3.3V LDO regulator is provided to power internal logic and external circuitry, such as the hall effect sensors or microcontroller, whose output capability is 50mA. A bypass capacitor between V3P3 pin and GND is required. The recommended value for the bypass capacitor is 4.7μF to 10μF.

Charge Pump

The charge pump is used to generate a gate supply which is greater than V_{IN} to turn on the high-side FETs. A 1μF (10V or higher) ceramic capacitor is required between VIN and VCP pins.

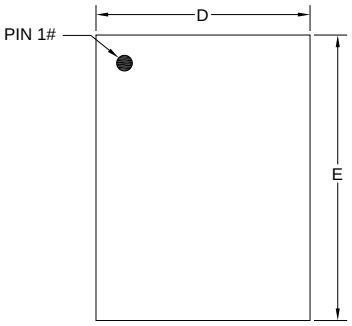
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

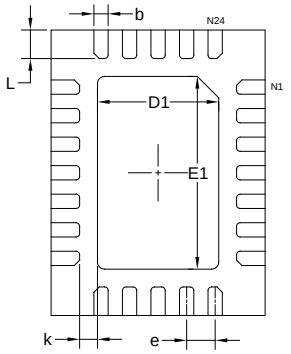
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

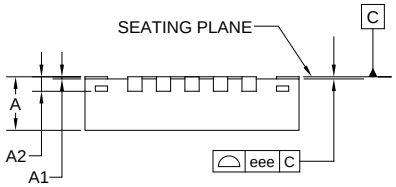
TQFN-3×4-24L



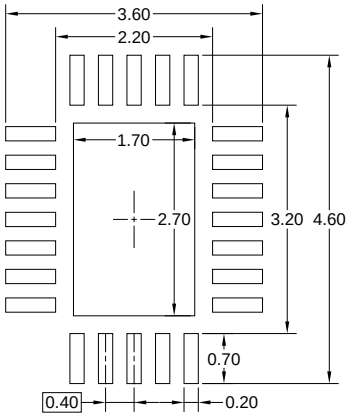
TOP VIEW



BOTTOM VIEW



SIDE VIEW



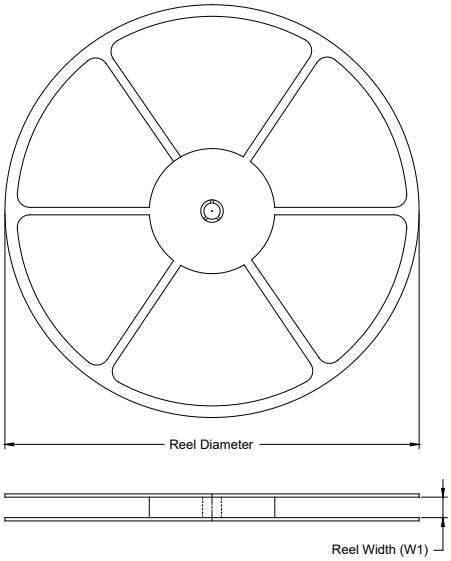
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	0.200	0.250
D	2.900	3.000	3.100
E	3.900	4.000	4.100
D1	1.600	1.700	1.800
E1	2.600	2.700	2.800
k	0.250 REF		
L	0.300	0.400	0.500
e	0.400 BSC		
eee	0.080		

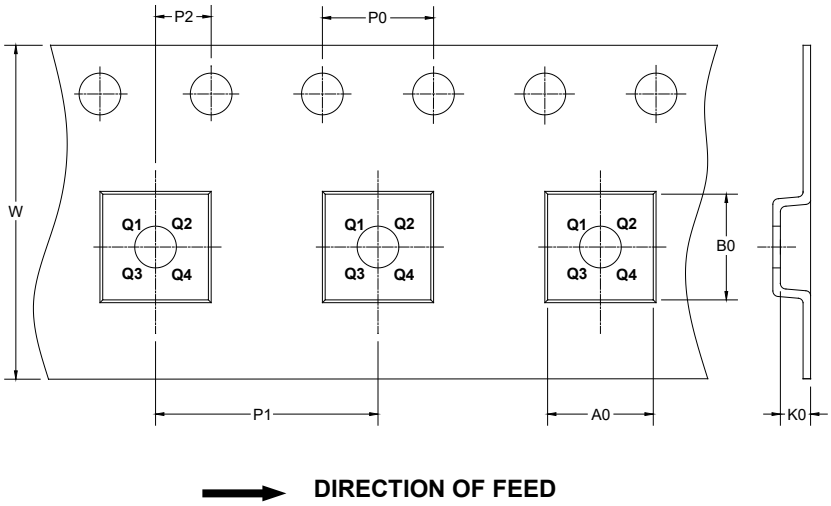
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



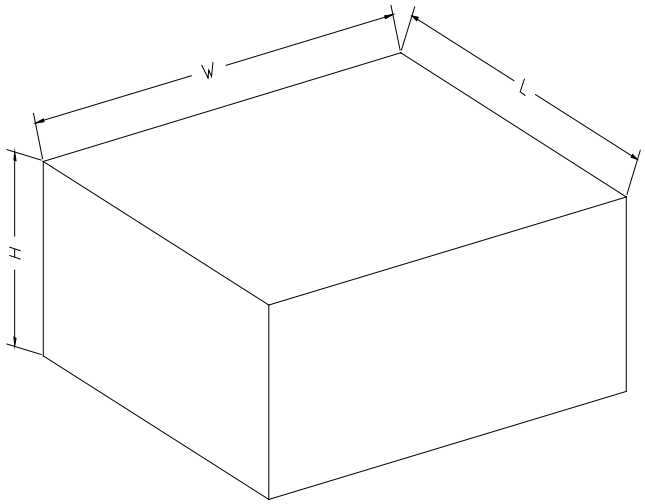
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-24L	13″	12.4	3.40	4.40	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002