SGMCD1020Q
22-Channel Multiple Switch Detection Interface for Automotive Applications

GENERAL DESCRIPTION

The SGMCD1020Q provides a low-cost integrated switch detection solution. As a multiple switch detection interface (MSDI) device, it can detect the switch status of up to 22 channels and transfer the switch status information (open or closed) to the microprocessor unit (MCU) through a serial peripheral interface (SPI). In addition, the device features a 22-to-1 analog multiplexer for outputting buffered selected input analog signals to the AMUX pin so that the signal can be read by the MCU.

The SGMCD1020Q has three modes of operation: normal mode, low-power mode (LPM) and polling mode. When the device is in normal mode, the device can be programmed and can provide the corresponding wetting current to the switch contacts as it monitors the switch status. During low-power mode, the low quiescent current makes the device ideal for applications in automotive or industrial scenarios that require low sleep state current. The polling mode periodically detects the input pins to determine their state and to determine if the state has changed from normal mode.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGMCD1020Q is available in a Green TQFN-5×5-32GL package. It operates over the junction temperature range of -40℃ to +125℃.

APPLICATIONS

Automotive Applications
Zoom Control Unit (ZCU)
Advanced Driver Assistance System (ADAS)
Central Gateway/In-Vehicle Networking
Lighting
Heating Ventilation and Air Conditioning (HVAC)
Gasoline Engine Management

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Full Functions Guaranteed: 6.0V ≤ V_{BATP} ≤ 36V**
- **Full Parameters Guaranteed: 6.0V ≤ V_{BATP} ≤ 28V**
- **Input Voltage Range of Switch: -1.0V to 36V**
- **8 Programmable Inputs (Switches to Battery or Ground)**
- **14 Switch-to-Ground Inputs**
- **4 Selectable Wetting Current Levels: 2mA, 8mA, 12mA and 16mA**
- **Use 3.3V/5.0V SPI Protocol to Communicate Directly with MCU**
- **Selectable Wake-up during Change-of-Switch State**
- **Typical Standby Current:**
  - **I_{BATP} = 70μA (TYP)**
  - **I_{VDDQ} = 4.4μA (TYP)**
- **Active Interrupt (INT_B) on Switch State Changing**
- **Available in a Green TQFN-5×5-32GL Package**

TYPICAL APPLICATION

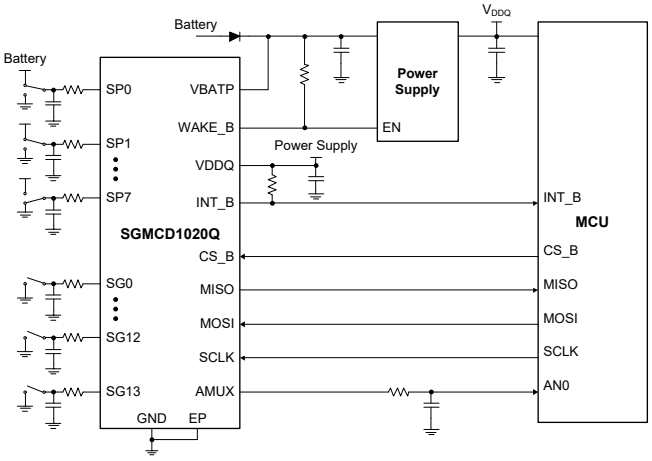


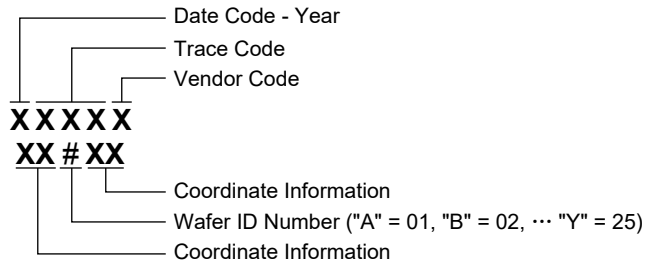
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMCD1020Q	TQFN-5×5-32GL	-40℃ to +125℃	SGMCD1020QTVP32G/TR	0T3TVP32 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Battery Voltage, V_{BATP} ..... -0.3V to 40V
Supply Voltage, V_{DDQ} ..... -0.3V to 7V
SPI Inputs/Outputs
CS_B, MOSI, MISO, SCLK ..... -0.3V to 7V
SGx, SPx Switch Input Voltage ..... -14V (1) to 38V
AMUX Voltage ..... -0.3V to 7V
INT_B Voltage ..... -0.3V to 7V
WAKE_B Voltage ..... -0.3V to 40V
Package Thermal Resistance
TQFN-5×5-32GL, θ_{JA} ..... 30.3℃/W
TQFN-5×5-32GL, θ_{JB} ..... 9.4℃/W
TQFN-5×5-32GL, $\theta_{JC(TOP)}$ ..... 17.3℃/W
TQFN-5×5-32GL, $\theta_{JC(BOT)}$ ..... 2.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
Contact Discharge (2)
VBATP (3) ..... ±8000V
WAKE_B (Series Resistor 10kΩ) ..... ±8000V
SGx/SPx Pins with 100nF Capacitor (Series Resistor 100Ω) ..... ±8000V
ESD Susceptibility (4) (5)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. Minimum value of -18V is guaranteed by design for switch input voltage range (SGx, SPx).

2. C_{ZAP} = 150pF, R_{ZAP} = 330Ω (Powered and Unpowered).

3. External component requirements at system level: reverse blocking diode from battery to VBATP (0.6V < V_F < 1V). See Figure 20.

4. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

5. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Battery Voltage, V_{BATP} ..... 6V to 36V
Supply Voltage, V_{DDQ} ..... 3V to 5.25V
SPI Inputs/Outputs
CS_B, MOSI, MISO, SCLK ..... 3V to 5.25V
SGx, SPx Switch Input Voltage ..... -1V to 36V
AMUX, INT_B Voltage ..... 0V to 5.25V
WAKE_B Voltage ..... 0V to 36V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

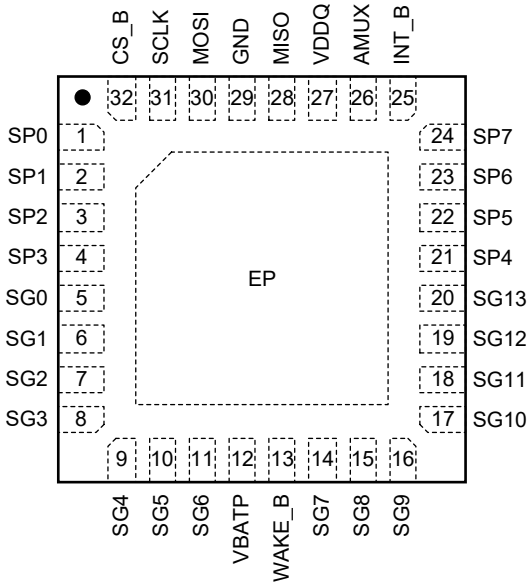
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5×5-32GL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1 ~ 4, 21 ~ 24	SP0 ~ SP3, SP4 ~SP7	I	Programmable Switch Inputs Pins. All of the 8 inputs can be programmed to either SB or SG.
5 ~ 11, 14 ~ 20	SG0 ~ SG6, SG7 ~SG13	I	Switch-to-Ground Inputs Pins.
12	VBATP	P	Battery Supply Input Pin. This pin requires an external reverse protection circuit.
13	WAKE_B	I/O	Open-Drain Wake-up Output Pin. It can be used as an enable pin to control external power supply. As an input, it can be used to wake device up from LPM due to external events.
25	INT_B	I/O	Open-Drain Output to MCU. Used as an indication when the change of switch status occurs. As an input, it can be used to wake device up from LPM due to external INT_B falling events.
26	AMUX	O	Analog Multiplex Output Pin.
27	VDDQ	I	3.3V/5.0V Supply Input Pin. Set SPI communication level.
28	MISO	O/SPI	Slave Output and Master Input Pin. Digital data of SGMCD1020Q out pin to MCU.
29	GND	G	Ground for Logic, Analog.
30	MOSI	I/SPI	Master Output and Slave Input Pin. Control Data of MCU input pin to SGMCD1020Q.
31	SCLK	I/SPI	Clock Input Pin.
32	CS_B	I/SPI	Chip Select Input Pin.
—	EP	G	It is recommended to connect the EP to GND and system ground.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DDQ} = 3.1V to 5.25V, V_{BATP} = 6V to 28V, T_A = -40℃ to +125℃, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Input						
VBATP Supply Power-on Reset Voltage	V_{BATP_POR}		2.7	3.3	3.8	V
VBATP Under-Voltage Rising Threshold	V_{BATP_UV}			4.3	4.6	V
VBATP Under-Voltage Hysteresis	$V_{BATP\_UV\_HYS}$		250		500	mV
VBATP Over-Voltage Rising Threshold	V_{BATP_OV}		32		37	V
VBATP Over-Voltage Hysteresis	$V_{BATP\_OV\_HYS}$		1.5		3	V
VBATP Supply Current	I_{BAT_ON}	All switches open, normal mode, tri-state disabled (all channels)		7	12	mA
VBATP Low-Power Mode Supply Current (Polling Disabled)	$I_{BATP\_IQ\_LPM\_P}$	V_{BATP} = 6V to 28V		70	105	μA
VBATP Polling Current (1)	$I_{POLLING\_IQ}$	Polling 64ms, all channels wake enabled		2		μA
Normal Mode VDDQ Current	I_{VDDQ_NOR}	SCLK, MOSI, WAKE_B = 0V, CS_B, INT_B = VDDQ, no SPI communication, AMUX selected no input			160	μA
Logic Low-Power Mode Supply Current	I_{VDDQ_LPM}	SCLK, MOSI = 0V, CS_B, INT_B, WAKE_B = VDDQ, no SPI communication		4.4	10	μA
VDDQ Under-Voltage Falling Threshold	V_{DDQ_UV}		2.2		2.8	V
VDDQ Under-Voltage Hysteresis	$V_{DDQ\_UV\_HYS}$		150		300	mV
Switch Input						
SGx/SPx Pins Leakage to GND	$I_{L\_SG\_GND}$	Inputs tri-stated, analog mux selected for each input, voltage at SGx = VBATP			3	μA
SGx/SPx Pins Leakage to Battery	$I_{L\_SG\_BAT}$	Inputs tri-stated, analog mux selected for each input, voltage at SGx = GND			2	μA
SG Sustain Current (3) (Mode 0 Wetting Current)	I_{SUS_SG}	V_{BATP} = 6V to 28V	1.60	2.00	2.40	mA
SB Sustain Current (Mode 0 Wetting Current)	I_{SUS_SB}		1.55	2.00	2.85	mA
SG and SB Wetting Current Level (3)	I_{WET}	Mode 1 = 8mA		8		mA
		Mode 2 = 12mA		12		
		Mode 3 = 16mA		16		
SG Wetting Current Tolerance (4)	I_{WET_SG}	Mode 1 to 3			14	%
SB Wetting Current Tolerance (5)	I_{WET_SB}	Mode 1 to 3			14	%
Switch Detection Threshold (6)	V_{IC_THR}		3.7	4.0	4.3	V
Switch Detection Threshold Low-Power Mode (SG only) (1) (7)	$V_{IC\_THR\_LPM}$		120	230	440	mV
Switch Detection Threshold Hysteresis	$V_{IC\_THR\_H}$	4V threshold	70		320	mV
Input Threshold 2.5V (Used for Comparator Only)	$V_{IC\_TH\_2P5}$		2	2.5	3	V
SG Low-Power Mode Polling Current	$I_{ACTIVE\_POLL\_SG}$	V_{BATP} = 6V to 28V	0.7	1.1	1.44	mA
SB Low-Power Mode Polling Current	$I_{ACTIVE\_POLL\_SB}$		1.5	2.1	2.85	mA
Digital Interface						
MISO Tri-State Leakage Current	I_{HZ}	V_{DDQ} = 0V to V_{DDQ}	-2		2	μA
SI, SCLK, CS_B, INT_B Input Logic Voltage Thresholds	V_{IN_LOGIC}		V_{DDQ} × 0.25		V_{DDQ} × 0.7	V
SI, SCLK, CS_B, INT_B Input Logic Hysteresis	$V_{IN\_LOGIC\_HYS}$		60			mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDQ} = 3.1V to 5.25V, V_{BATP} = 6V to 28V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WAKE_B Input Logic Voltage Threshold	$V_{IN\_LOGIC\_WAKE}$		1.2	1.6	2.0	V
WAKE_B Input Logic Voltage Hysteresis	$V_{IN\_WAKE\_HYS}$		150		650	mV
SCLK/MOSI Input Current	I_{SCLK}, I_{MOSI}	SCLK/MOSI = 0V	-2		2	μA
SCLK/MOSI Pull-Down Current	I_{SCLK}, I_{MOSI}	SCLK/MOSI = VDDQ	15		50	μA
CS_B Input Current	I_{CS_BH}	CS_B = VDDQ	-2		2	μA
CS_B Pull-up Resistor to VDDQ	R_{CS_BL}	CS_B = 0V	60	120	190	kΩ
MISO High-side Output Voltage	V_{OH_MISO}	I_{OHMISO} = -1mA	V_{DDQ} - 0.8		V_{DDQ}	V
MISO Low-side Output Voltage	V_{OL_MISO}	I_{OLMISO} = 1mA			0.4	V
Input Capacitance on SCLK, MOSI, Tri-State MISO	C_{IN}			5		pF
Analog MUX Output						
Input Offset Voltage When Selected as Analog (2) (8)	V_{OS}	ES suffix	-15		15	mV
Analog Operational Amplifier Output Voltage	V_{OL_AMUX}	Sink 1mA			70	mV
Analog Operational Amplifier Output Voltage	V_{OH_AMUX}	Source 1mA	V_{DDQ} - 0.15			V
INT_B						
INT_B Output Low Voltage	V_{OL_INT}	I_{OUT} = 1mA		0.2	0.4	V
INT_B Output High Voltage	V_{OH_INT}	INT_B = Open-circuit	V_{DDQ} - 0.5		V_{DDQ}	V
Pull-up Resistor to VDDQ	R_{PU}		65	120	180	kΩ
Leakage Current INT_B	$I_{LEAK\_INT\_B}$	INT_B pulled up to VDDQ			2	μA
Temperature Limit						
Temperature Warning	T_{FLAG}	First flag to trip	105	115	135	℃
Temperature Monitor (8)	T_{LIM}		156	165	174	℃
Temperature Monitor Hysteresis (8)	T_{LIM_HYS}		6	11	16	℃
WAKE_B						
WAKE_B Voltage Low	$V_{WAKE\_B\_VOL}$	WAKE_B = 1.0mA (R_{PU} to V_{BATP} = 16V)			0.3	V
WAKE_B Voltage High	$V_{WAKE\_B\_VOH}$	WAKE_B = open-circuit	V_{DDQ} - 0.7		V_{DDQ}	V
WAKE_B Internal Pull-up Resistor to VDDQ	$R_{WAKE\_B\_RPU}$		100	150	200	kΩ
WAKE_B Leakage	$I_{WAKE\_B\_LEAK}$	WAKE_B pulled up to V_{BATP} = 16V through 10kΩ			2	μA

NOTES:

1. Guaranteed by design.
2. The AMUX output voltage deviates from the selected input voltage, when there is a negative voltage on the other SGx/SPx pins.
3. When V_{BATP} is low, the SG wetting current may be limited due to the small headroom between V_{BATP} and SG pin voltage.
4. (I_{SUS_MAX} - I_{SUS_MIN}) × 100/I_{SUS_MIN}.
5. (I_{WET_MAX} - I_{WET_MIN}) × 100/I_{WET_MIN}.
6. Switch detection threshold decreases when V_{BATP} is lower than 6V.
7. When SPx pins are programmed as SB during LPM, the only wake-up detection comparator threshold V_{IC_THR} is 4V.
8. Guaranteed by characterization during the design period, not verified via final testing.

DYNAMIC CHARACTERISTICS

(V_{DDQ} = 3.1V to 5.25V, V_{BATP} = 6V to 28V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
POR to Active Time	t_{ACTIVE}	Under-voltage to normal mode	260	370	490	μs
Switch Input						
Normal Mode Pulse Wetting Current Timer	t_{PULSE_ON}		16.5	20	24	ms
Normal Mode Interrupt Delay Time	$t_{INT-DLY}$		5		25	μs
Low-Power Mode Polling Timer Accuracy	$t_{POLLING}$				10	%
SG Active Polling Timer	$t_{ACTIVE\_POLL\_SG}$		38	56	70	μs
SB Active Polling Timer	$t_{ACTIVE\_POLL\_SB}$	SBPOLL TIME = 0	1	1.2	1.4	ms
		SBPOLL TIME = 1	38	56	70	μs
Input Glitch Filter Timer	t_{GLITCH}	Normal mode	5		25	μs
AMUX Output						
AMUX Access Time (Tri-State to On)	$t_{AMUX\_VALID\_TS}$	C_{MUX} = 1nF, rising edge of CS_B to selected			20	μs
Oscillator						
Oscillator Tolerance	$t_{OSC\_TOL\_LPM}$	f = 192kHz, low-power mode	-10		10	%
	$t_{OSC\_TOL\_NOR}$	f = 4.0MHz, normal mode	-15		15	%
Interrupt						
INT Pulse Duration	t_{INT_PULSE}	Interrupt occurs or INT_B request	80	110	135	μs
SPI Interface (1)						
Transfer Frequency	f_{OP}				8	MHz
SCLK Period	t_{SCK}		160			ns
Enable Lead Time	t_{LEAD}		140			ns
Enable Lag Time	t_{LAG}		50			ns
SCLK High Time	t_{SCK_HS}		56			ns
SCLK Low Time	t_{SCK_LS}		56			ns
MOSI Input Setup Time	t_{SUS}		16			ns
MOSI Input Hold Time	t_{HS}		20			ns
MISO Access Time	t_A				116	ns
MISO Disable Time	t_{DIS}				100	ns
MISO Output Valid Time	t_{VS}				62	ns
MISO Output Hold Time (No Cap on MISO)	t_{HO}		10			ns
Rising Time	t_{RO}				40	ns
Falling Time	t_{FO}				40	ns
CS_B Negated Time	t_{CSN}		500			ns
WAKE-UP						
LPM Mode Wake-up Time Triggered by Edge of CS_B (2)	$t_{CSB\_WAKE-UP}$			480		μs

NOTES:
1. All SPI timing is performed with a 100pF load on MISO, unless otherwise noted.
2. The parameter is guaranteed when V_{BATP} is within the range from 6V to 28V.

TIMING DIAGRAM

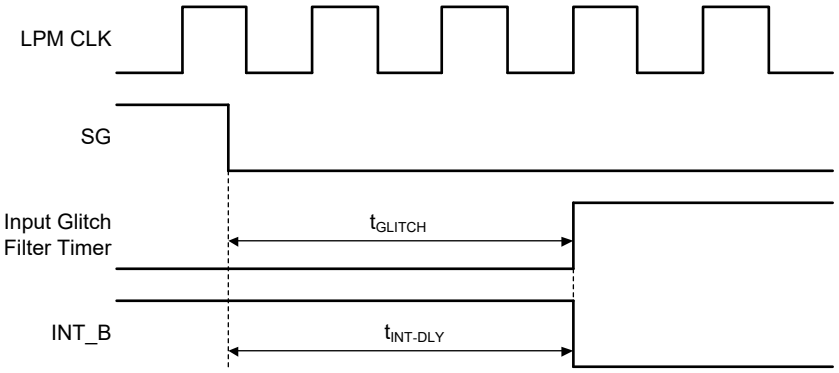


Figure 2. Glitch Filter and Interrupt Delay Timers

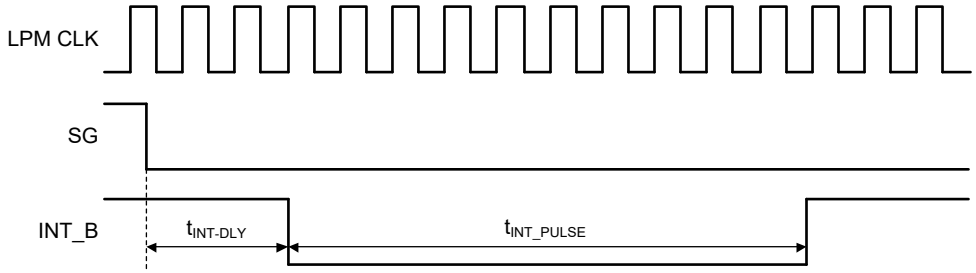


Figure 3. Interrupt Pulse Timer

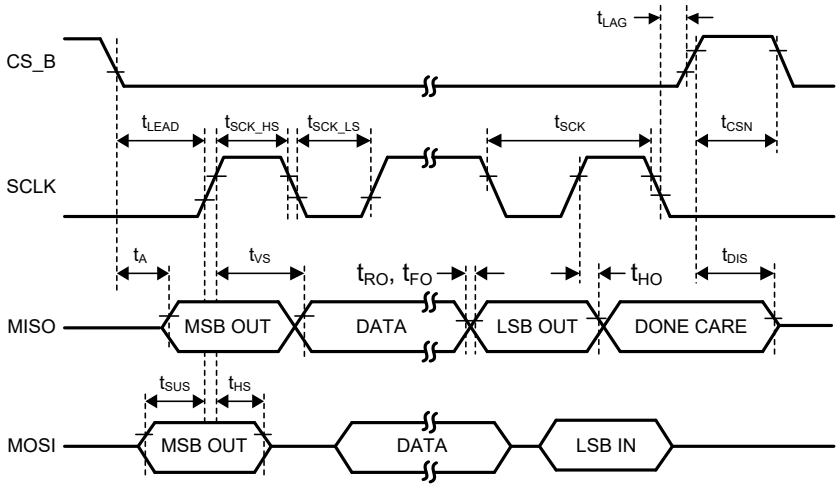


Figure 4. SPI Timing Diagram

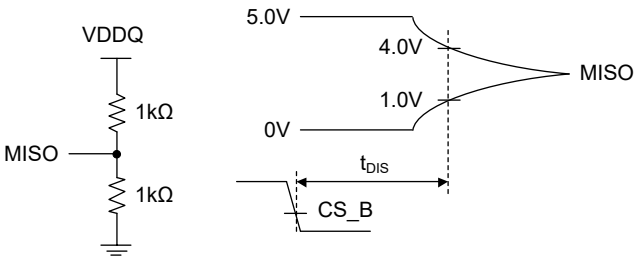
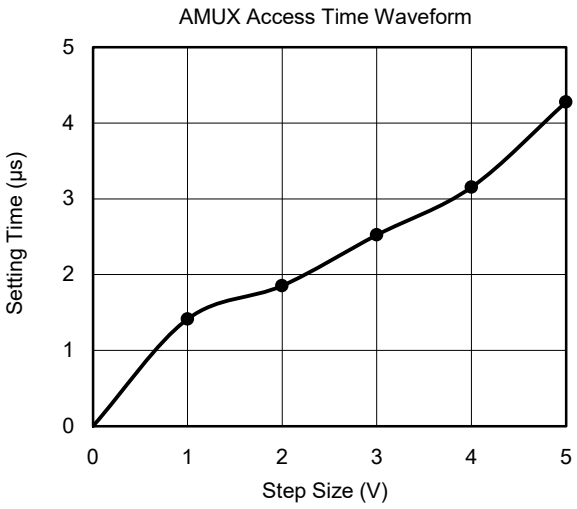


Figure 5. MISO Loading for Disable Time Measurement

TYPICAL PERFORMANCE CHARACTERISTICS

V_{BATP} = 12V, V_{DDQ} = 5V.



FUNCTIONAL BLOCK DIAGRAM

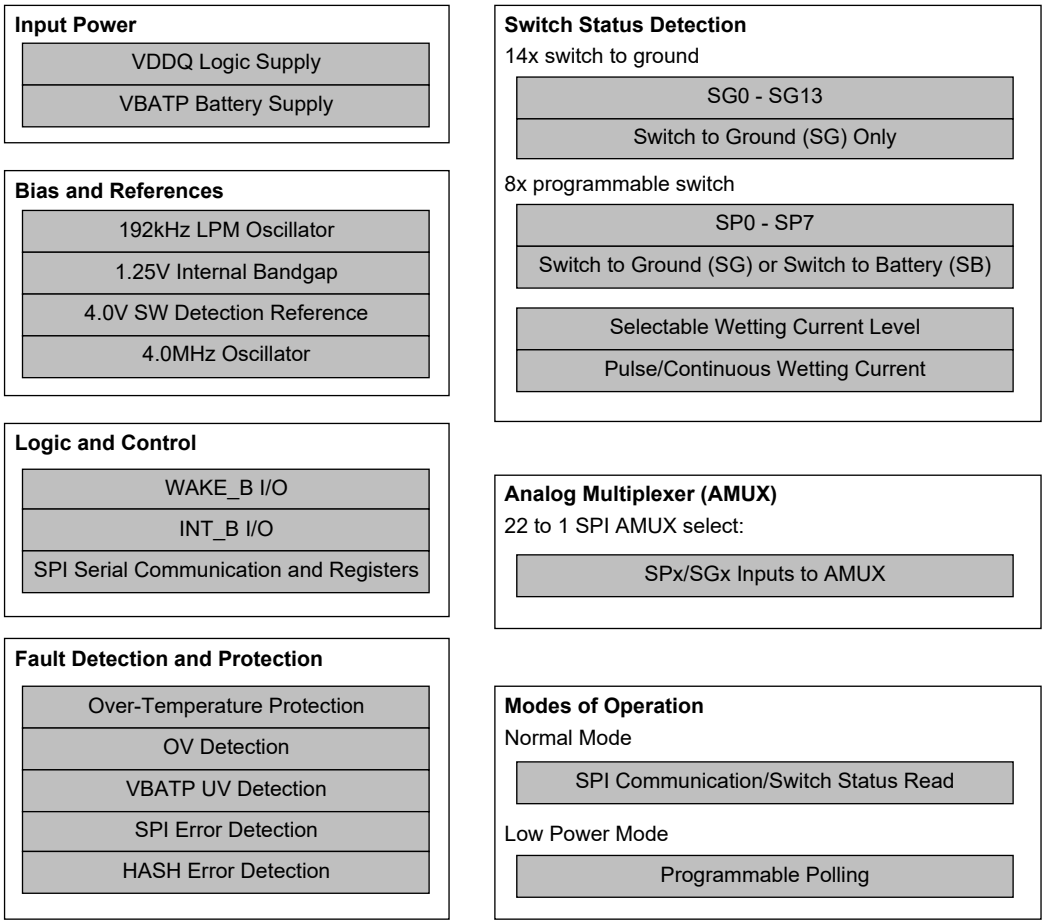


Figure 6. Functional Block Diagram

INTERNAL BLOCK DIAGRAM

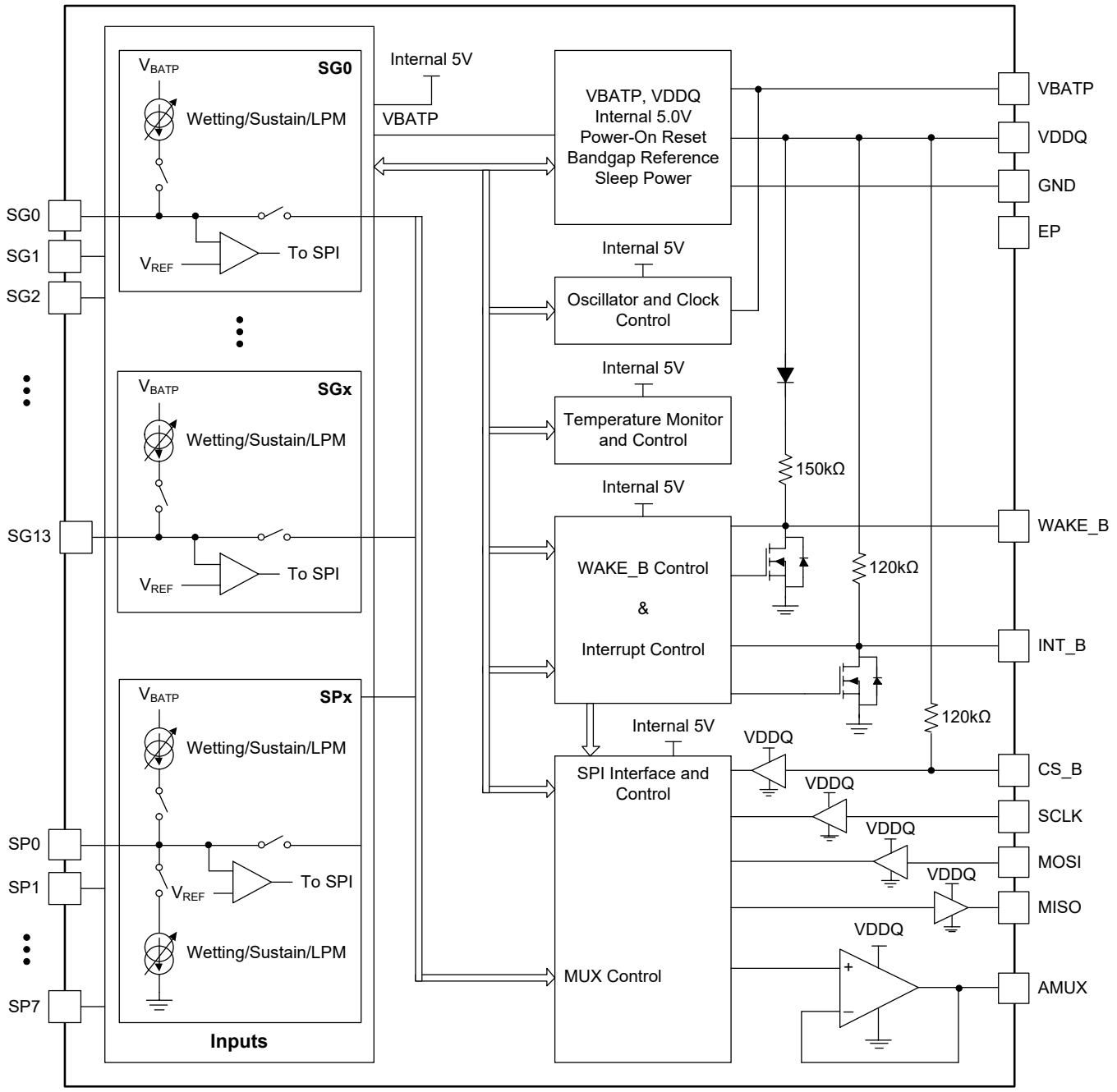


Figure 7. Internal Block Diagram

DETAILED DESCRIPTION

General IC Functional Description

The SGMCD1020Q is a multiple switch detection interface (MSDI) which can detect the switch status change of 14 switch-to-ground (SG) inputs and 8 switch-to-power (SP) inputs. The SP input can be configured as switch-to-battery (SB) input or SG input through the internal registers. The device uses the serial peripheral interface (SPI) to communicate with the microcontroller unit (MCU) and transfers the switch status of either open or closed. The SGMCD1020Q also has an analog multiplexer, called AMUX, to obtain the SP/SG channel voltages information and buffers it for the possible reading requirement from the MCU.

The SGMCD1020Q needs an RC network at each SP/SG input in order to mitigate the pulse impingement. Besides, an anti-reverse diode in the forward path from the supply source to the VBATP pin is needed as well. As for the SP/SG channels, no external anti-reverse diode is needed due to the existence of internal one provided by the SGMCD1020Q.

Battery Voltage Ranges

The VBATP pin operating voltage ranges from 6V to 36V. The maximum voltage is 40V and external supply source voltage higher than 40V should be limited to 40V, or the device might be permanently damaged. Besides, an anti-reverse diode in the forward path from the supply source (such as a battery) to the VBATP pin is needed.

Load Dump (Over-Voltage)

If a load dump event occurs, the VBATP pin voltage will increase and may exceed the device over-voltage threshold of 32V. Once an over-voltage event occurs, the wetting current is reduced to 2mA and registers are locked. In this condition, no switch status change is detected and no fault is reported unless the device comes back to normal mode.

Jump Start (Double Battery)

During a jump start (double battery) condition, the SGMCD1020Q functions normally with all parameters listed in Electrical Characteristics section. No internal faults are set and no abnormal operation noted as a result of operating in this range.

Normal Battery Range

The SGMCD1020Q functions normally with all parameters listed in Electrical Characteristics section.

Under-Voltage

In the under-voltage range, the SPI can communicate with the MCU, but errors may occur.

Under-Voltage Lockout

In the under-voltage lockout range, the SPI communication is prohibited. That is, MISO pin will not transmit any data to the MCU, and CS_B pin will not receive any pulse from the MCU. When an under-voltage lockout event occurs at any point of communication process, the device responds immediately and enters the under-voltage lockout mode at once. An SPI bit is reserved to indicate whether the device has just left the under-voltage lockout mode.

Power-on Reset (POR) Activated

During the POR ranges of 2.7V to 3.8V, the SPI communication is prohibited and all register bits are reset to the default ones. When the VBATP pin voltage rises above the POR region, the SGMCD1020Q begins to enable the SPI communication and refresh all the register values to the default ones (see SPI Control register). Once a POR event occurs and after that the VBATP pin voltage falls into the normal mode range, an SPI bit in Device Configuration register will indicate the POR event.

No Operation

The device does not function and no switch detection is possible.

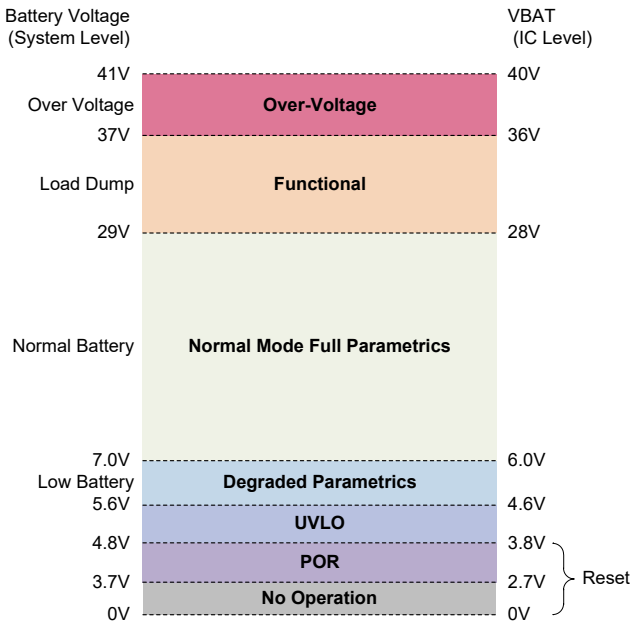


Figure 8. Battery Voltage Range

DETAILED DESCRIPTION (continued)

Power Sequencing Conditions

The SGMCD1020Q contains two power supply pins: VBATP and VDDQ. VBATP pin provides power for the internal sources and SG related power supplies, while VDDQ pin provides power for the SPI communication related pins (CS_B, SCLK, MISO, MOSI, AMUX), and indicated pins (INT_B, WAKE_B). The following describes the SGMCD1020Q performance under different timing sequence for VBATP and VDDQ.

V_{BATP} before V_{DDQ}

Usually, the user should power VBATP first and power VDDQ in the next. Once the VBATP pin is powered ready, the internal sources are in normal operation and logic states are all in the default settings. The SPI communication function and indicated pins will be active as soon as the VDDQ pin is powered ready.

V_{DDQ} before V_{BATP}

Sometimes VDDQ may be applied before or without VBATP power. Thanks for the isolation between the VABTP powered circuits and the VDDQ powered circuits, no current can flow from the VDDQ pin to the VBATP pin so that the device may turns on. However, if the VBATP is powered after VDDQ, the SGMCD1020Q outputs definite logic state after t_{ACTIVE} (POR to active time).

V_{BATP} Ready, V_{DDQ} Lost

In this scenario, the current logic state is maintained, while SPI communication is unavailable.

V_{DDQ} Ready, V_{BATP} Lost

In this scenario, SPI communication is functional, while the actual logic state is undefined.

State Diagram

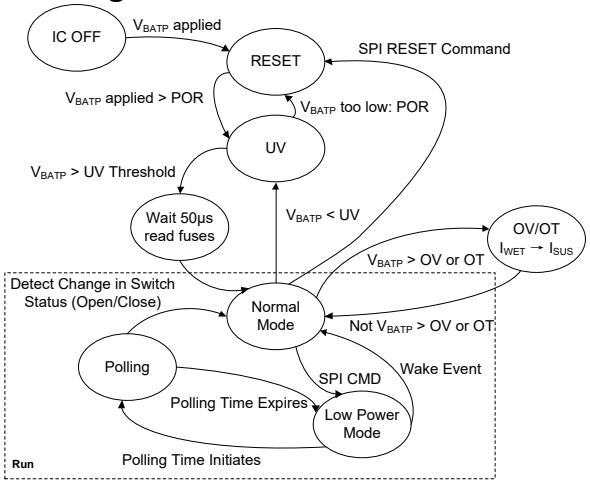


Figure 9. SGMCD1020Q State Diagram

State Machine

Figure 9 shows the state machine operation logic. When VBATP voltage is lower than POR, all registers are in the default settings and no SPI communication is permitted.

UV: Under-Voltage Lockout

Once the POR circuit has reset the device, the SGMCD1020Q enters the UV state. In this particular state, the IC retains all register settings; however, it is in a lockout mode, which means that no SPI communication is permitted. The analog multiplexer (AMUX) is inactive, and the current sources are deactivated. Since the MISO is disabled in this state, the user will not obtain a valid response from it. The chip oscillators, which operate at 4.0MHz for most normal mode and 192kHz for low-power mode (LPM), are activated during the UV state. When the VBATP voltage ascends above the UV threshold (approximately rising threshold of 4.3V), the SGMCD1020Q begins to read fuses state after 50µs.

Normal Mode

Under normal mode, the device enables SPI communication with the MCU, AMUX reading, switch status detection and related configurations including settings of wetting current, detection threshold and interrupt generated from switch state change. Note that not all registers in LPM are activated in normal mode and that any LPM-related registers is not permitted setting under LPM. In other words, LPM registers must be set under normal mode. Besides, all fault events, including OV, OT, temp flag warning, SPI error, can be reported in this mode.

Low-Power Mode

The SGMCD1020Q provides the low-power mode (LPM) in order to greatly reduce the supply current. The user has only one way to enter the LPM: writing to the Enter Low-Power Mode register. WAKE_B is used to indicate whether the device is in LPM. Once in LPM, most power rails, 4.0MHz oscillator and all fault detection function are closed. That means no fault report is recorded in LPM.

DETAILED DESCRIPTION (continued)

Polling Mode

The SGMCD1020Q operates in a polling mode. It periodically (with the period being selectable in LPM Configuration register) checks the input pins to figure out their states and ascertains if there has been a switch state change since the chip was in normal mode. There are multiple configurations available for this mode, providing the user with enhanced operational flexibility. In this mode, the current sources are utilized to either pull-up (for SG) or pull-down (for SB) in order to determine whether a switch is open or closed. More details can be found in the Low-Power Mode Operation section.

When the VBATP voltage is low, the polling process is halted and it waits until the VBATP rises above the under-voltage (UV) level or a POR event takes place. The polling pause guarantees that all internal power rails, currents, and thresholds reach the necessary levels for precisely detecting open or closed switches. In this situation, the chip does not wake up; it merely waits for the VBATP voltage to increase or for a POR to occur.

Once the polling concludes, the device can be reverted to LPM or enter the normal mode if detecting a wake event. And the CS_B, INT_B and WAKE_B (configurable) events can also wake it. In the LPM or polling mode, the comparator only mode switch detection is constantly active. Changing the state of those inputs will effectively wake up the IC in polling mode.

If wake-up enable bits are disabled on all SG and SP channels, the device will not respond to state changes on any input pins. In this case, the polling timer is turned off to achieve the lowest current consumption in low-power mode. The device will then disable the polling timer to allow for minimum current consumption in low-power mode.

Low-Power Mode Operation

The current consumption in LPM is the lowest for SGMCD1020Q. The user has only one way to enter the LPM: writing to the Enter Low-Power Mode register. The register settings are the same with those under normal mode.

The user has several ways to exit LPM and enter normal mode:

- Change of input switch state (when enabled)
- Falling edge of WAKE_B (as set by Device Configuration register of the device)
- Falling edge of INT_B (V_{DDQ} = 5.0V)
- Falling edge of CS_B (V_{DDQ} = 5.0V)
- Power-on Reset (POR)

In LPM, it is possible to remove the V_{DDQ} supply from the device. When V_{DDQ} is removed, a wake-up triggered by the falling edge of INT_B and CS_B will be disabled. After a falling edge occurs on WAKE_B (as selected in the Device Configuration register) INT_B, or CS_B, the device examines V_{DDQ} status. If V_{DDQ} is low, the IC goes back to LPM without reporting a wake-up event. If V_{DDQ} is high, the IC wakes up and reports the event. Additionally, when the device is awakened using CS_B, the first MISO data message is invalid.

The LPM command includes the polling timer setting, which periodically monitors the inputs in low-power mode to detect any state changes. The t_{ACTIVE_POLL} duration indicates the time that the device remains active within each polling cycle to check for state changes. The LPM voltage threshold enables the user to decide based on the balance between noise immunity and the lower current levels that polling allows. Figure 8 illustrates the polling process.

If an input is determined to be open when entering LPM, and remains open during a polling event, the chip will stop the polling event for that particular input (or those inputs) in order to reduce the current consumption. Figure 11 shows that SG and SB are logically the same in this regard.

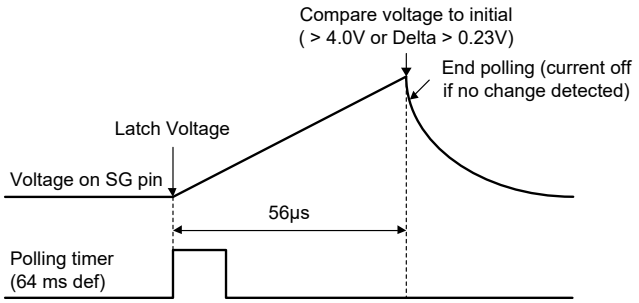


Figure 10. Low-Power Mode Polling Check

DETAILED DESCRIPTION (continued)

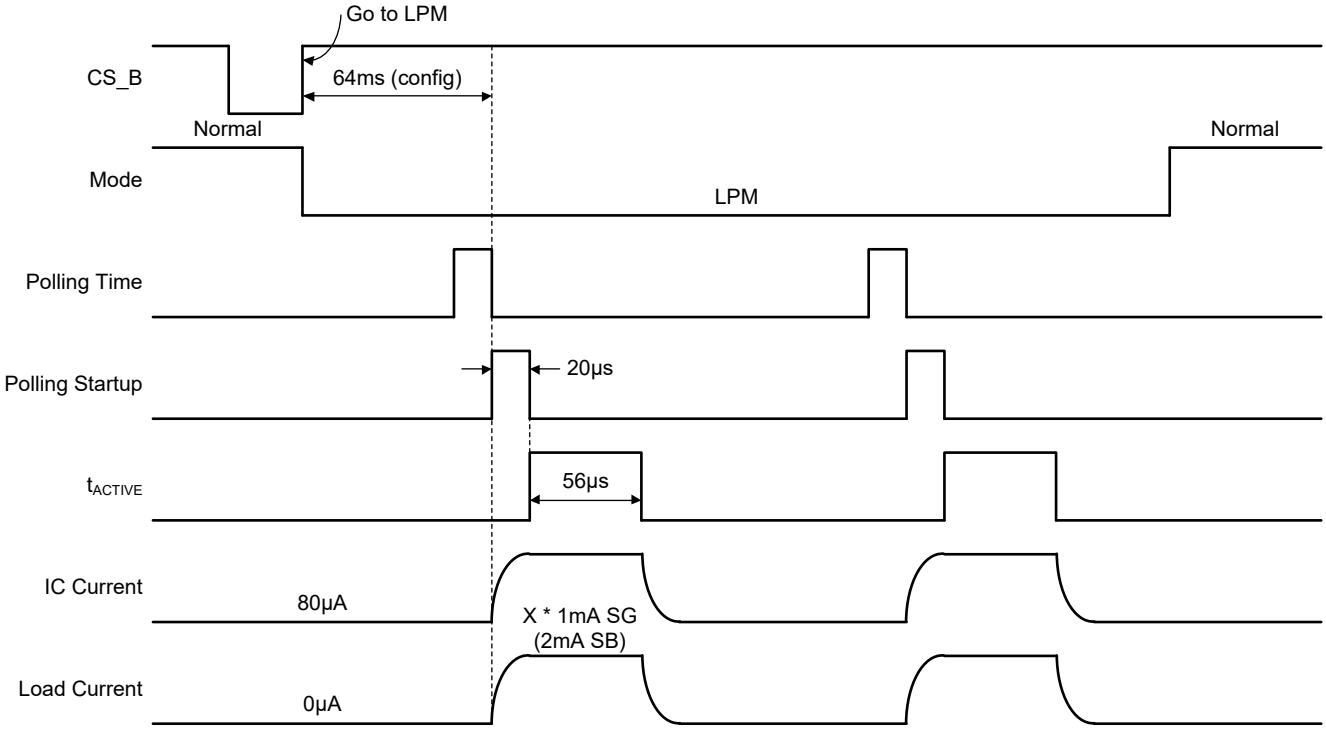


Figure 11. Low-Power Mode Typical Timing

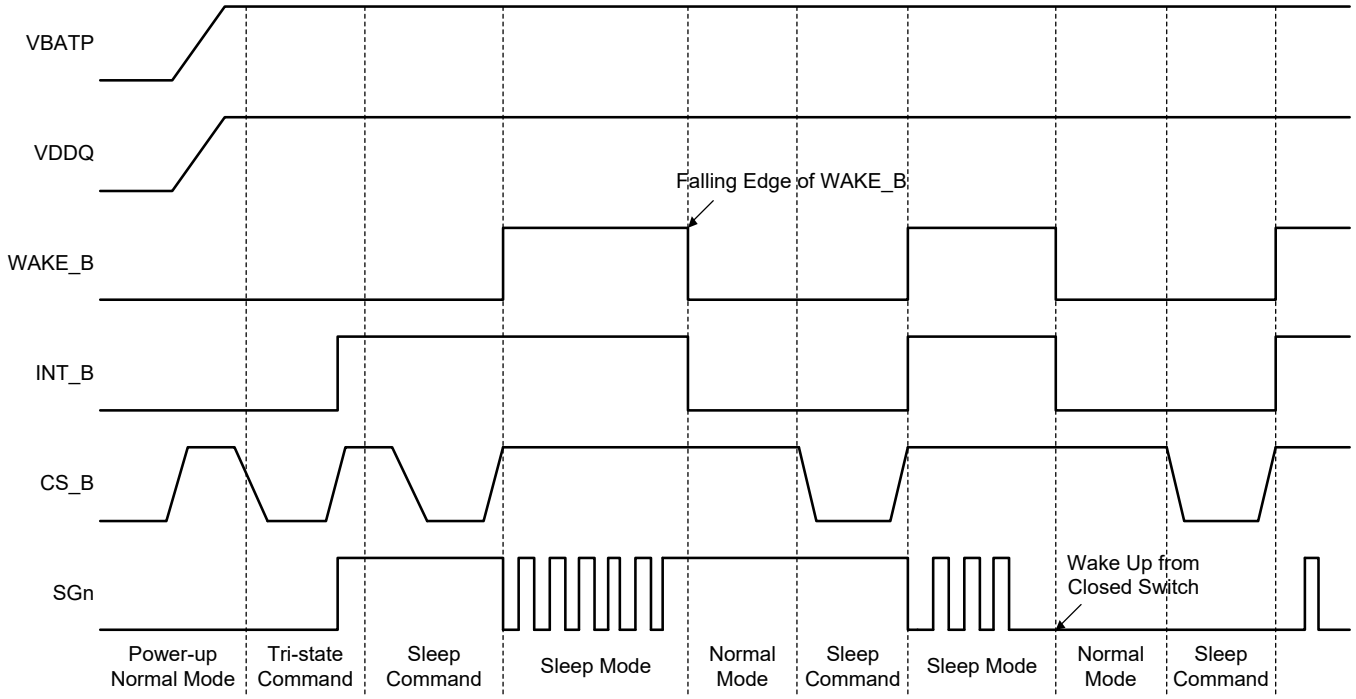


Figure 12. Low-Power Mode to Normal Mode Operation

DETAILED DESCRIPTION (continued)

Input Functional Block

The SG pins function only as switch-to-ground inputs and are equipped with pull-up current sources. The SP pins, on the other hand, can be configured either as switch-to-ground (SG) or switch-to-battery (SB) with both pull-up and pull-down current sources.

The input is contrasted against a 4.0V reference (the input comparator threshold is configurable). For SG pins, voltages exceeding the input comparator threshold value are regarded as open, while for SB configuration, they are considered as closed. Conversely, voltages lower than the input comparator threshold values are deemed closed for SG pins and open for SB configurations. Programming characteristics are detailed in the SPI Control Register section.

The input comparator owns hysteresis for the thresholds and those are determined by the closing action of the switch (falling for SG, rising for SB). Employing numerous inputs with continuous wetting current levels will lead to overheating of the IC and might trigger an over-temperature (OT) event.

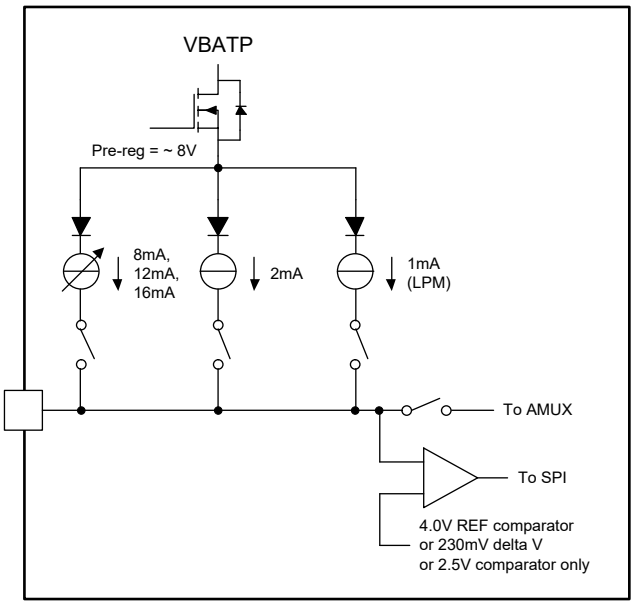


Figure 13. SG Block Diagram

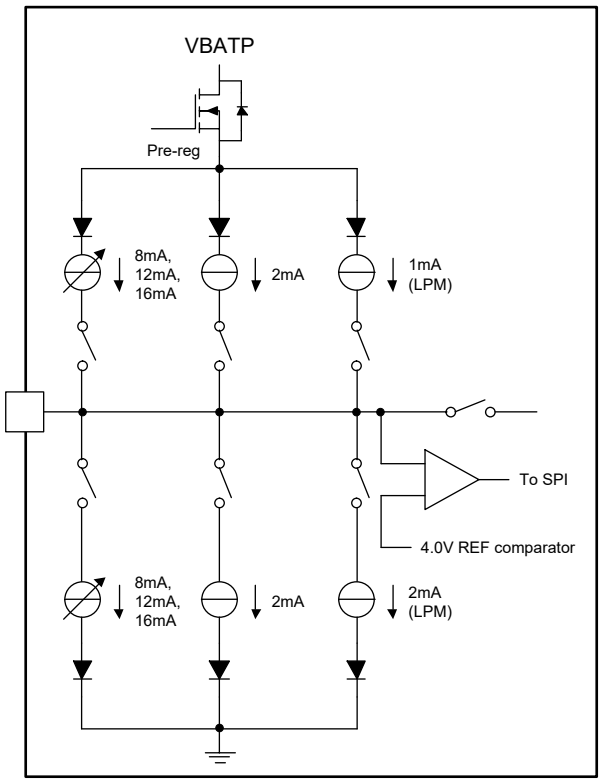


Figure 14. SP Block Diagram

Oscillator and Timer Control Functional Block

The SGMCD1020Q has two basic oscillators: a 4.0MHz oscillator and a 192kHz oscillator. These two oscillators create all other clocks. Note that the 4.0MHz oscillator works under normal mode while both the 4.0MHz oscillator and the 192kHz oscillator work under LPM. The accuracy value of 4.0MHz oscillator is ±15%, while the 192kHz oscillator is ±10%.

Temperature Monitor and Control Functional Block

The SGMCD1020Q possesses several thermal detection cells to monitor the temperature outside. These cell outputs are OR-ed and then sent to the MCU. The device gives a temperature warning flag bit (rising threshold of +115℃) and OT monitoring bit (rising threshold of +165℃ with hysteresis of 11℃). Once an OT event occurs, the wetting current is forced to be 2mA unless the temperature drops below T_{LIM} - T_{LIM_HYS} typically.

DETAILED DESCRIPTION (continued)

WAKE_B Control Functional Block

The WAKE_B pin can be considered as an open-drain output or a wake-up input. WAKE_B keeps low in the normal mode, and will be pulled high in LPM. The WAKE_B features an internal pull-up to VDDQ and an internal series diode, enabling an external pull-up to VBATP if needed.

When WAKE_B is used as an input, and is pulled high in LPM. A low command from the MCU triggers the falling edge of WAKE_B, pushing the device in normal mode. If VDDQ goes low in LPM, the WAKE_B pin can still activate the device based on the setting of the WAKE_B bit in the Device Configuration register. This enables the user to pull the WAKE_B pin up to VBATP, allowing its use in a VDDQ-lost configuration.

When WAKE_B is used as an output, it can drive either an MCU input or the Enable_B of a regulator (potentially for VDDQ). In the normal mode, the WAKE_B is driven low regardless of the state of VDDQ. In LPM, the WAKE_B is released and is expected to be pulled up either internally to VDDQ or externally to VBATP. Once a valid wake-up event is detected, the device wakes up from LPM, WAKE_B signal is set low, irrespective of the VDDQ condition.

INT_B Functional Block

The INT_B pin serves as both an input and an output. It indicates that an interrupt event has taken place and can also receive interrupts from other devices when multiple INT_B pins are connected in a wired-OR configuration. The INT_B pin is an open-drain output with an internal pull-up to VDDQ. In the normal mode, a change in the switch state triggers the INT_B pin (provided that it is enabled). The INT_B pin and the INT_B bit in the SPI register are latched when the CS_B pin has a falling edge. This enables the MCU to identify the source of the interrupt. When two SGMCD1020Q devices are utilized, only the device that initiates the interrupt will have its INT_B bit set. The INT_B pin and the INTflg bit are cleared 1μs after the falling edge of CS_B. If a switch contact change occurs while CS_B is low, the INT_B pin will not clear when CS_B has a rising edge.

In a system with multiple SGMCD1020Q devices, where WAKE_B is high and VDDQ is on in LPM, the falling edge of INT_B causes the device to enter the normal mode. The INT_B pin can be configured to have either a pulsed output (where it is pulsed low for a specific INT pulse duration) or a latched-low output. The default setting is the latched-low operation, and the pulsed option can be selected via the SPI.

The MCU can request an INT_B operation by sending a SPI word, which will result in a low pulse of 110μs duration on the INT_B pin. The chip causes an INT_B assertion for the following cases:

- Switch state change
- Any Wake-up event
- Fault events like OV, OT, etc.
- POR

AMUX Functional Block

The MCU can read the analog voltage of a switch by SPI commands. Inside the IC, there is a 22-to-1 analog multiplexer, called AMUX. The AMUX pin can output the voltage potential on SG/SP pins which is selected by the chip. No matter how high the voltage of input pin is, the output voltage on AMUX pin will be limited to the given value of VDDQ. The value of the matching bit in the next MISO data stream will be logic ‘0’ after choosing an input as the analog. The current level of the AMUX output can be set by users when they need to select a channel to be read as analog input. It is supported to set current level to the programmed wetting current or high impedance for the selected channel. When an input is selected to be sent to AMUX pin, there is no polling current on the input pin and the chip cannot wake up from state change in low-power mode. Before entering low-power mode, it is recommended to set the AMUX to ‘no input selected’ state. The buffer function is not available in the low-power mode.

Serial Peripheral Interface (SPI)

The SGMCD1020Q uses the SPI to communicate with the MCU. The SPI has four pins: SPI clock (SCLK), master-in slave-out (MISO), master-out slave-in (MOSI) and chip-selection bar (CS_B). The SGMCD1020Q is viewed as a slave unit for the SPI.

DETAILED DESCRIPTION (continued)

The SGMCD1020Q takes 32-bit data transmission rule to communicate with the MCU without recognizing modulo 0. Data that to be input without modulo 32-bit will be prohibited from sending into the chip. It adopts hash method to check whether the register value is true with the preset one. If not, an interrupt is issued out from the SPI and will be read by the MCU. The SPI support a daisy chain structure for multi-device communication function as well. Details can be seen from Figure 18.

Chip Select Low (CS_B)

The CS_B pin is used to choose which device is to be selected for communication. When the CS_B pin goes low, the MISO pin exits the tri-state mode, and all status information gets latched within the SPI Shift register. While the CS_B input is in the asserted state, register data is shifted into the MOSI pin and then shifted out from the MISO pin with each subsequent SCLK pulse. When the CS_B pin has a rising edge, the MISO pin returns to the tri-state mode, and the fault register is reloaded (latched) with the current filtered status data. In order to provide enough time for the fault registers to be reloaded properly, the CS_B pin must stay low for at least t_{CSN} before it goes high again.

The CS_B input is equipped with a pull-up current source connected to VDDQ. This is designed so that in case of an open-circuit condition, it can command the de-asserted state. Moreover, this pin has voltages with compatible thresholds, which enables it to operate properly with microprocessors that use a supply voltage ranging from 3.3V to 5.0V.

Serial Clock (SCLK)

The SCLK input serves as the clock signal, which is crucial for synchronizing the serial data transfer. This pin features threshold-compatible voltages, enabling it to operate correctly with microprocessors that utilize a supply voltage ranging from 3.3V to 5.0V.

When the CS_B input is in the asserted state (active low), both the Master MCU and this device latch input data when the SCLK has a rising edge. Typically, the SPI master shifts data out during the falling edge of SCLK, whereas this device shifts data out on the rising edge of SCLK. This is done to allow more time for driving the MISO pin to the appropriate level.

This SCLK input is also employed as the input for validating the module 32-bit counter. In the event that any SPI transmissions are not exact multiples of 32 bits (in other words, not exact multiples of clock edges), such transmissions are regarded as illegal. In such cases, the entire frame is aborted and no changes are made to the information in the configuration or control registers.

Serial Data Output (MISO)

The MISO pin goes into the tri-state mode when CS_B is asserted low. As soon as CS_B step into the low impedance, the MISO state is identical to that of the MSB and sends out the data from the MSB to the LSB. The MISO high level voltage is nearly the same as that of VDDQ pin.

Serial Data Input (MOSI)

The MOSI pin receives data from the master MCU when CS_B is asserted low. It is compatible with voltages ranging from 3.3V to 5.0V for the VDDQ pin.

SPI CONTROL REGISTER

The user can use the SPI to configure the settings and read the current status of each input for the SGMCD1020Q. Besides, the SPI provides the Fault Status and INTflg bits for the MCU reading. Table 1 gives the detailed descriptions about the SPI MOSI registers.

Table 1. MOSI Input Register Bit Definition

Register #	Register Name	Address	TYPE
0	SPI Check	0000 000	R
02/03	Device Configuration Register	0000 001	R/W
04/05	Tri-State SP Register	0000 010	R/W
06/07	Tri-State SG Register	0000 011	R/W
08/09	Wetting Current Level SP Register	0000 100	R/W
0A/0B	Wetting Current Level SG Register 0	0000 101	R/W
0C/0D	Wetting Current Level SG Register 1	0000 110	R/W
16/17	Continuous Wetting Current SP Register	0001 011	R/W
18/19	Continuous Wetting Current SG Register	0001 100	R/W
1A/1B	Interrupt Enable SP Register	0001 101	R/W
1C/1D	Interrupt Enable SG Register	0001 110	R/W
1E/1F	Low-Power Mode Configuration	0001 111	R/W
20/21	Wake-up Enable Register SP	0010 000	R/W
22/23	Wake-up Enable Register SG	0010 001	R/W
24/25	Comparator Only SP	0010 010	R/W
26/27	Comparator Only SG	0010 011	R/W
28/29	LPM Voltage Threshold SP Configuration	0010 100	R/W
2A/2B	LPM Voltage Threshold SG Configuration	0010 101	R/W
2C/2D	Polling Current SP Configuration	0010 110	R/W
2E/2F	Polling Current SG Configuration	0010 111	R/W
39	Enter Low-Power Mode	0011 100	W
3A/3B	AMUX Control Register	0011 101	R/W
3E	Read Switch Status	0011 111	R
42	Fault Status Register	0100 001	R
47	Interrupt Request	0100 011	W
49	Reset Register	0100 100	W

Bit Types:
R: Read only; W: Write only; R/W: Read/Write
Read: 0; Write: 1

SPI CONTROL REGISTER (continued)

The SPI word of SGMCD1020Q is 32 bits made up of an 8-bit command word and three configuration words. The 8-bit command word is used to choose the specific configuration action, while the rest 24 bits are used to configure the individual inputs of SP/SG.

The SPI Configuration registers can be read or written to.

In order to read a register, send an SPI word with '0' in the LSB of the command word so that the relative register data will be sent to the MISO buffer in the next SPI cycle. Once a new READ command is sent out, the MISO gives the control word (READ) and its register data.

A READ example:

Send: 0x3E00 0000
Receive: 4800 0000 (for example after a POR)
Send: 0x0000 0000
Receive: 3E00 3FFF (address + register data)

The SGMCD1020Q reads the switch status after POR through the Read Status register with 0x3Exx xxxx. Exiting the LPM is similar. Details are presented in Figure 17.

In order to write a register, send an SPI word with '1' in the LSB of the command word and 24 individual input configurations to the rest 24 bits, so that the relative register address and three configuration words will be sent to the MISO buffer in the next SPI cycle. Details are presented in Figure 15.

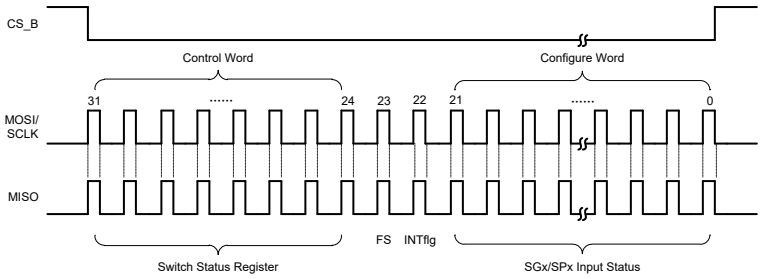


Figure 15. First SPI Operation (after POR)

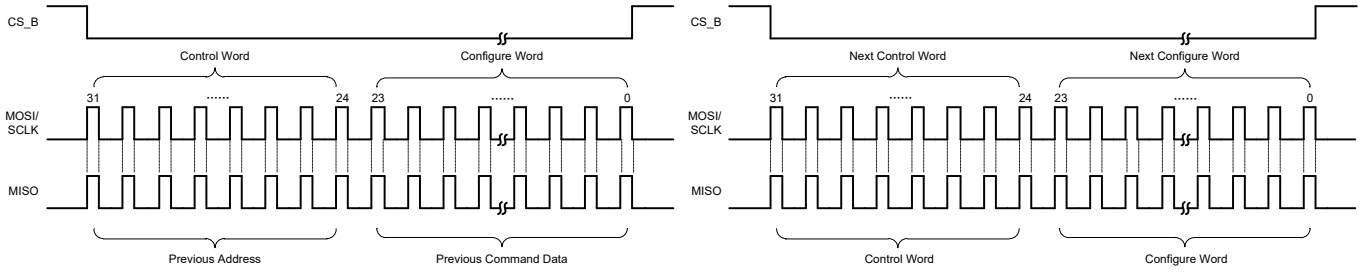


Figure 16. SPI Write Operation

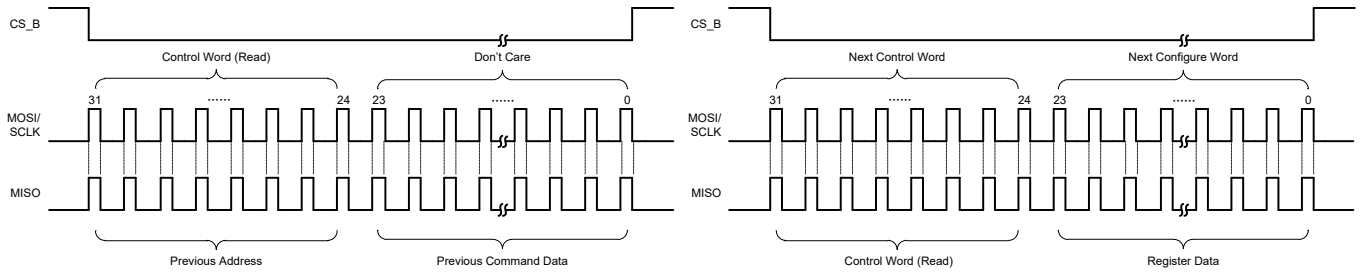


Figure 17. SPI Read Operation

SPI CONTROL REGISTER (continued)

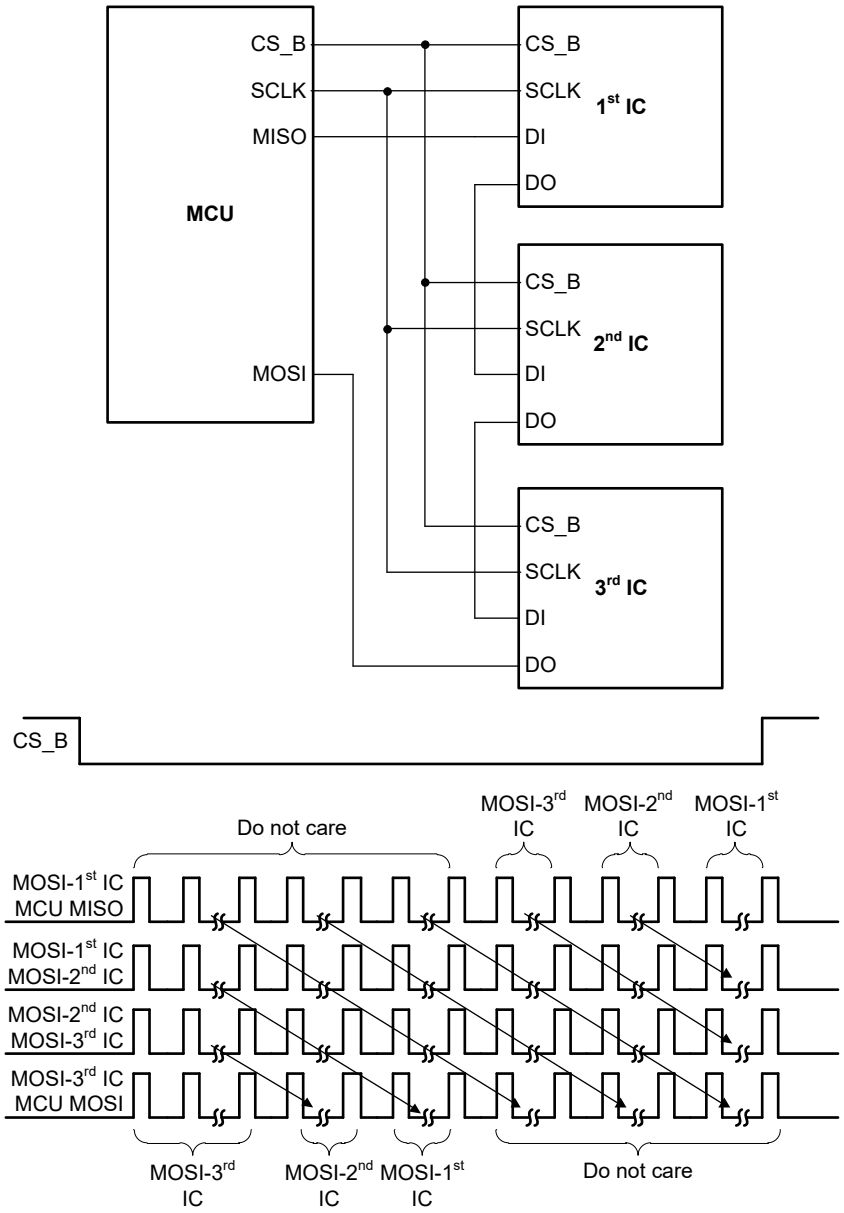


Figure 18. Daisy Chain SPI Operation

Register # 0: SPI Check Register

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R	0000 000	The SGMCD1020Q provides an option to test whether the device is ready via sending command with the SPI Check register. When reading this register, the received data will be 0x123456 under the correct operation of SGMCD1020Q. And it has no ability to report fault event or interrupt activity. Thus, all interrupt flag will be unchanged after this command. MISO Return Word: 0x00123456
D[24]	TYPE	R	0	
D[23:0]	SPI Check	R	0x000000	

SPI CONTROL REGISTER (continued)

Register # 02/03: Device Configuration Register

The device comes with several configuration settings that are of a global nature. Here are the details of these configuration settings:

In the situation where the SGMCD1020Q is within the OV region, if the VBATP OV bit is set to '0', the wetting current on all input channels will be limited to 2mA, and the device will not be able to enter low-power mode. On the other hand, when the VBATP OV bit is '1', the device can operate normally even when in the over-voltage region. It is important to note that the OV flag will be set whenever the device enters the over-voltage region, regardless of the value of the VBATP OV bit.

WAKE_B can serve the purpose of enabling an external power supply regulator to supply the VDDQ voltage rail. When the WAKE_B VDDQ check bit is '0', it's expected that the WAKE_B pin will be pulled up either internally or externally to VDDQ, and it's also anticipated that VDDQ will go low. As a result, the SGMCD1020Q will not wake up when there is a falling edge on the WAKE_B pin. However, when the WAKE_B VDDQ check bit is '1', it is assumed that the user is using an external pull-up to either VBATP or VDDQ (in cases where VDDQ is not expected to be off), and the SGMCD1020Q will wake up when there is a falling edge on the WAKE_B pin.

The INT_B out setting is used to determine how the INT_B pin functions when an interrupt occurs. The IC has the ability to either pulse low '1' or latch low '0'.

The inputs SP0 to SP7 can be programmed to be either switch-to-battery or switch-to-ground. These input types are defined through the settings command. To configure an SP input as switch-to-battery, the appropriate bit must be set to '1'. To set an SP input as SG, the appropriate bit must be set to '0'. In normal mode, the MCU can change or update the programmable switch register via software at any time. Irrespective of the setting, when the SP input switch is closed, logic '1' will be placed in the serial output response register.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 001	MISO Return Word: 0000 001[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13]	SBPOLL TIME	R/W	0	Set the active polling time for SP channel when it is configured as SB. 0 means the polling time is 1.2ms, while 1 means the polling time is 56μs.
D[12]	VBATP OV Disable	R/W	0	VBATP Over-Voltage Protection. 0 = Enabled 1 = Disable
D[11]	WAKE_B VDDQ Check	R/W	1	Decide whether the falling edge of the WAKE_B pin can exit the LPM if VDDQ is low. 0 = WAKE_B is pulled up to VDDQ and the falling edge of the WAKE_B pin cannot exit the LPM if VDDQ is low. 1 = WAKE_B is externally pulled up to VBATP or VDDQ, and the falling edge of the WAKE_B pin can make the device drop out from the LPM no matter what the VDDQ voltage is (V_{DDQ} is not expected to go low).
D[10]	INT_B OUT	R/W	0	Interrupt Pin Behavior. 0 = INT pin goes low and latched when an interrupt occurs until the SPI communicates. 1 = INT pin turns low shortly and then returns high.
D[9:8]	RESERVED	R/W	00	Reserved
D[7:0]	SP[7:0]	R/W	1111 1111	Configure the SP pin as Switch to Battery (SB) or Switch to ground (SG). 0 = Switch to Ground 1 = Switch to Battery

SPI CONTROL REGISTER (continued)

Register # 04/05: Tri-State SP Register

This register is intended to set the SP inputs as high impedance mode (tri-state) or not. Set the corresponding bit to '1' if a specific input is desired to be high impedance. In this condition, the 4V comparator is active and no wetting current is available. Set the corresponding bit to '0' if a specific input is not desired to be high impedance so that different level of wetting current can be configured. The default value for each SP channel is '1'. Note that every input that set to be in tri-state is still polled in the LPM. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 010	MISO Return Word: 0000 010[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	1111 1111	0 = Not tri-state. 1 = Tri-state.

Register # 06/07: Tri-State SG Register

This register is intended to set the SG inputs as high impedance mode (tri-state) or not. Set the corresponding bit to '1' if a specific input is desired to be high impedance. In this condition, the 4V comparator is active and no wetting current is available. Set the corresponding bit to '0' if a specific input is not desired to be high impedance so that different level of wetting current can be configured. The default value for each SG channel is '1'. Note that every input that set to be in tri-state is still polled in the LPM. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 011	MISO Return Word: 0000 011[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x3FFF	0 = Not tri-state. 1 = Tri-state.

Register # 08/09: Wetting Current Level SP Register

This register is intended to set the wetting current level (2mA, 8mA, 12mA and 16mA) for the SP inputs. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 100	MISO Return Word: 0000 100[0/1]
D[24]	TYPE	R/W	0/1	
D[23:21]	SP7[2:0]	R/W	110	Wetting Current Levels Selection. 000 = 2mA 010 = 8mA 100 = 12mA 110 = 16mA (Default)
D[20:18]	SP6[2:0]	R/W	110	
D[17:15]	SP5[2:0]	R/W	110	
D[14:12]	SP4[2:0]	R/W	110	
D[11:9]	SP3[2:0]	R/W	110	
D[8:6]	SP2[2:0]	R/W	110	
D[5:3]	SP1[2:0]	R/W	110	
D[2:0]	SP0[2:0]	R/W	110	

SPI CONTROL REGISTER (continued)

Register # 0A/0B: Wetting Current Level SG Register 0

This register is intended to set the wetting current level (2mA, 8mA, 12mA and 16mA) for the SG inputs. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 101	MISO Return Word: 0000 101[0/1]
D[24]	TYPE	R/W	0/1	
D[23:21]	SG7[2:0]	R/W	110	Wetting Current Levels Selection. 000 = 2mA 010 = 8mA 100 = 12mA 110 = 16mA (Default)
D[20:18]	SG6[2:0]	R/W	110	
D[17:15]	SG5[2:0]	R/W	110	
D[14:12]	SG4[2:0]	R/W	110	
D[11:9]	SG3[2:0]	R/W	110	
D[8:6]	SG2[2:0]	R/W	110	
D[5:3]	SG1[2:0]	R/W	110	
D[2:0]	SG0[2:0]	R/W	110	

Register # 0C/0D: Wetting Current Level SG Register 1

This register is intended to set the wetting current level (2mA, 8mA, 12mA and 16mA) for the SG inputs. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0000 110	MISO Return Word: 0000 110[0/1]
D[24]	TYPE	R/W	0/1	
D[23:18]	RESERVED	R/W	0000 00	Bit 23: Fault Status Bit 22: INTflg
D[17:15]	SG13[2:0]	R/W	110	Wetting Current Levels Selection. 000 = 2mA 010 = 8mA 100 = 12mA 110 = 16mA (Default)
D[14:12]	SG12[2:0]	R/W	110	
D[11:9]	SG11[2:0]	R/W	110	
D[8:6]	SG10[2:0]	R/W	110	
D[5:3]	SG9[2:0]	R/W	110	
D[2:0]	SG8[2:0]	R/W	110	

Register # 16/17: Continuous Wetting Current SP Register

For each switch input, there is a specific 20ms timer assigned to it. The timer kicks off when the particular switch input goes beyond the comparator threshold. Once the 20ms time period elapses, the contact current will drop from the configured wetting current, which is 16mA, down to the sustain current (2mA). The wetting current is designed to be at a relatively high level initially and will decrease to the lower sustain current level once the timer has run out. In cases where multiple wetting current timers are disabled, it is essential to take the power dissipation into account.

In the normal mode, the MCU can modify or update the Continuous Wetting Current register by using software at any time. This gives the MCU the power to control how long the wetting current is applied to the switch contact. When the continuous wetting current bit is set to ‘0’, it functions in the typical way where a higher wetting current is applied first, and then after 20ms, the sustain current comes into play (this is called the pulsed wetting current operation). However, if this bit is programmed to ‘1’, it activates the continuous wetting current, leading to a full-time wetting current level. By default, the Continuous Wetting Current register is set to ‘0’, which means it operates in the pulse wetting current operation mode.

SPI CONTROL REGISTER (continued)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0001 011	MISO Return Word: 0001 011[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	0000 0000	0 = Pulsed wetting current. 1 = Continuous wetting current.

Register # 18/19: Continuous Wetting Current SG Register

Every switch input is associated with a specific 20ms timer. This timer begins counting down when the particular switch input surpasses the comparator threshold. Once the 20ms timer reaches its expiration time, the contact current is decreased from the initially configured wetting current level, which is 16mA, down to 2.0mA. The wetting current is set at a relatively high level initially and then reduces to the lower sustain current level after the timer has elapsed. When multiple wetting current timers are disabled, it is necessary to take the power dissipation into account.

In normal mode, the MCU has the ability to modify or update the Continuous Wetting Current register through software at any time. This empowers the MCU to regulate the duration for which the wetting current is applied to the switch contact. When the continuous wetting current bit is programmed to ‘0’, the operation proceeds in the usual manner where a higher wetting current is applied first, followed by the sustain current after 20ms (this is known as pulse wetting current operation). On the other hand, programming this bit to ‘1’ activates the continuous wetting current, resulting in a full-time wetting current level. By default, the Continuous Wetting Current register is set to ‘0’, which corresponds to the pulse wetting current operation.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0001 100	MISO Return Word: 0001 100[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x0000	0 = Pulsed wetting current. 1 = Continuous wetting current.

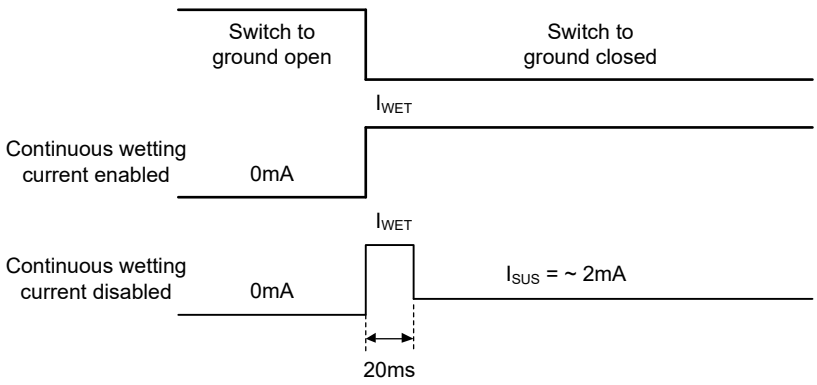


Figure 19. Pulsed/Continuous Wetting Current Configuration

SPI CONTROL REGISTER (continued)

Register # 1A/1B: Interrupt Enable SP Register

This register determines whether an interrupt will be issued under an event of switch status change. Set the corresponding bit to '1' if an interrupt is desired to be issued. Set the corresponding bit to '0' if no interrupt is desired to be issued. The default value for all SP inputs is '1'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0001 101	MISO Return Word: 0001 101[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	1111 1111	0 = Disable an interrupt from a specific switch change. 1 = Enable an interrupt from a specific switch change.

Register # 1C/1D: Interrupt Enable SG Register

This register determines whether an interrupt will be issued under an event of switch status change. Set the corresponding bit to '1' if an interrupt is desired to be issued. Set the corresponding bit to '0' if no interrupt is desired to be issued. The default value for all SG inputs is '1'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0001 110	MISO Return Word: 0001 110[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x3FFF	0 = Disable an interrupt from a specific switch change. 1 = Enable an interrupt from a specific switch change.

Register # 1E/1F: Low-Power Mode Configuration Register

This register is intended to set the polling period in LPM with four bits. The register value can be changed by the MCU at any time.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0001 111	MISO Return Word: 0001 111[0/1]
D[24]	TYPE	R/W	0/1	
D[23:4]	RESERVED	R/W	0x00000	Bit 23: Fault Status Bit 22: INTflg
D[3:0]	POLL[3:0]	R/W	1111	Set the polling rate for switch detection. 0000 = 3.0ms 0001 = 6.0ms 0010 = 12ms 0011 = 24ms 0100 = 48ms 0101 = 68ms 0110 = 76ms 0111 = 128ms 1000 = 32ms 1001 = 36ms 1010 = 40ms 1011 = 44ms 1100 = 52ms 1101 = 56ms 1110 = 60ms 1111 = 64ms (default)

SPI CONTROL REGISTER (continued)

Register # 20/21: Wake-up Enable SP Register

This register is intended to decide whether the SP inputs can wake up the SGMCD1020Q from the LPM or not. Set the corresponding bit to '1' if a specific input is desired to make the SGMCD1020Q exit the LPM. Set the corresponding bit to '0' if a specific input is not desired to wake up from the LPM. The default value for each SP channel is '1'. Note that the polling timer is closed once all the SP/SG inputs are unable to wake up the device from the LPM for the purpose of lower supply current. The register value can be changed by the MCU at any time in normal mode.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 000	MISO Return Word: 0010 000[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x00	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	1111 1111	0 = Disable specific input from waking up the device. 1 = Enable specific input from waking up the device.

Register # 22/23: Wake-up Enable SG Register

This register is intended to decide whether the SG inputs can wake up the SGMCD1020Q from the LPM or not. Set the corresponding bit to '1' if a specific input is desired to make the SGMCD1020Q exit the LPM. Set the corresponding bit to '0' if a specific input is not desired to wake up from the LPM. The default value for each SG channel is '1'. Note that the polling timer is closed once all the SP/SG inputs are unable to wake up the device from the LPM for the purpose of lower supply current. The register value can be changed by the MCU at any time in normal mode.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 001	MISO Return Word: 0010 001[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x3FFF	0 = Disable specific input from waking up the device. 1 = Enable specific input from waking up the device.

Register # 24/25: Comparator Only SP Register

This register is intended to provide comparator threshold of 2.5V with no polling current under the LPM. Set the corresponding bit to '1' if a specific input is desired to use this comparator threshold without polling current. Set the corresponding bit to '0' if a specific input is not desired to use this function. The default value for each SP channel is '0'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 010	MISO Return Word: 0010 010[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	0000 0000	0 = Disable the input comparators with threshold of 2.5V. 1 = Enable the input comparators with threshold of 2.5V in LPM with no polling current.

SPI CONTROL REGISTER (continued)

Register # 26/27: Comparator Only SG Register

This register is intended to provide comparator threshold of 2.5V with no polling current under the LPM. Set the corresponding bit to '1' if a specific input is desired to use this comparator threshold without polling current. Set the corresponding bit to '0' if a specific input is not desired to use this function. The default value for each SG channel is '0'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 011	MISO Return Word: 0010 011[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x0000	0 = Disable the input comparators with threshold of 2.5V. 1 = Enable the input comparators with threshold of 2.5V in LPM with no polling current.

Register # 28/29: LPM Voltage Threshold Configuration SP Register

This register is intended to set the voltage threshold used under LPM for SP inputs. Set the corresponding bit to '1' if a specific input of SP which is chosen as SG is desired to adopt the normal threshold of 4V (V_{IC_THR}). Otherwise, set the corresponding bit to '0' if a specific input of SP which is chosen as SG is desired to adopt the delta voltage threshold of 230mV ($V_{IC\_THR\_LPM}$). The default value for each SP channel is '0'. Note that every SP input that set to SB can only take the normal threshold of 4V as the voltage threshold used under LPM. Be careful with the voltage crossing between the open state and closed state and choose the suitable wetting current level under LPM.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 100	MISO Return Word: 0010 100[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	0000 0000	0 = Use the LPM delta voltage thresholds of 230mV and 4V to judge the switch status. 1 = Use the normal voltage threshold of 4V to judge the switch status.

Register # 2A/2B: LPM Voltage Threshold Configuration SG Register

This register is intended to set the voltage threshold used under LPM for SG inputs. Set the corresponding bit to '1' if a specific input of SG is desired to adopt the normal threshold of 4V (V_{IC_THR}). Otherwise, set the corresponding bit to '0' if a specific input of SG is desired to adopt the delta voltage threshold of 230mV ($V_{IC\_THR\_LPM}$). The default value for each SG channel is '0'. Be careful with the voltage crossing between the open state and closed state and choose the suitable wetting current level under LPM.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 101	MISO Return Word: 0010 101[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x0000	0 = Use the LPM delta voltage threshold of 230mV and 4V to judge the switch status. 1 = Use the normal voltage threshold of 4V to judge the switch status.

SPI CONTROL REGISTER (continued)

Register # 2C/2D: Polling Current Configuration SP Register

This register is intended to set the polling wetting current level for SP inputs under the LPM. Set the corresponding bit to '1' if a specific input is desired to take the wetting current level configured in Wetting Current Level SP register, Wetting Current Level SG register 0 and Wetting Current Level SG register 1. Set the corresponding bit to '0' if a specific input is desired to use the default polling wetting current level (2mA for SB and 1mA for SG). The default value for each SP channel is '0'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 110	MISO Return Word: 0010 110[0/1]
D[24]	TYPE	R/W	0/1	
D[23:8]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[7:0]	SP[7:0]	R/W	0000 0000	0 = Set each input normal polling current under LPM. 2mA polling current for SB configuration and 1mA polling current for SG configuration. 1 = Take the wetting current setting in Wetting Current Level Registers as the polling current value in LPM.

Register # 2E/2F: Polling Current Configuration SG Register

This register is intended to set the polling wetting current level for SP inputs under the LPM. Set the corresponding bit to '1' if a specific input is desired to take the wetting current level configured in Wetting Current Level SP register, Wetting Current Level SG register 0 and Wetting Current Level SG register 1. Set the corresponding bit to '0' if a specific input is desired to use the default polling wetting current level of 1mA. The default value for each SG channel is '0'.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0010 111	MISO Return Word: 0010 111[0/1]
D[24]	TYPE	R/W	0/1	
D[23:14]	RESERVED	R/W	0000 0000 00	Bit 23: Fault Status Bit 22: INTflg
D[13:0]	SG[13:0]	R/W	0x0000	0 = Set each input normal polling current under LPM. 2mA polling current for SB configuration and 1mA polling current for SG configuration. 1 = Take the wetting current setting in Wetting Current Level Registers as the polling current value in LPM.

Register # 39: Enter Low-Power Mode Register

This register is intended to enter the LPM. Note that this register is written only. When exiting from the LPM, all register settings are unchanged and the fault status is fed back. Also, the INTflg bit is put high and all SP/SG channel states are returned.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	W	0011 100	MISO Return Word: —
D[24]	TYPE	W	1	
D[23:0]	LPM	W	0x000000	

Register # 3A/3B: AMUX Control Register

This register is intended to select one of the SP/SG channel and transfer the voltage information to the AMUX pin for the MCU to read. The selected channel will not be checked for switch state change and the next SPI command for MISO is '0'. Note that the AMUX output pin is buffered and can be configured as tri-state or not through the ASETT0 bit. If the ASETT0 bit is '1', then programmable wetting current level may help the user to read sensor inputs. Besides, the AMUX pin is clamped to VDDQ irrespective of how large the SP/SG voltage is. The default value for channel selection is '000000' (none). The register value can be changed by the MCU at any time.

SPI CONTROL REGISTER (continued)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R/W	0011 101	MISO Return Word: 0011 101[0/1]
D[24]	TYPE	R/W	0/1	
D[23:7]	RESERVED	R/W	0x0000	Bit 23: Fault Status Bit 22: INTflg
D[6]	ASETT0	R/W	0	AMUX Current (Z_{SOURCE}) Select. 0 = Hi-Z (default) 1 = I_{WET}
D[5:0]	ASEL[5:0]	R/W	000000	AMUX Channel Select. 000000 = No Input Selected 000001 = SG0 000010 = SG1 000011 = SG2 000100 = SG3 000101 = SG4 000110 = SG5 000111 = SG6 001000 = SG7 001001 = SG8 001010 = SG9 001011 = SG10 001100 = SG11 001101 = SG12 001110 = SG13 001111 = SP0 010000 = SP1 010001 = SP2 010010 = SP3 010011 = SP4 010100 = SP5 010101 = SP6 010110 = SP7

Register # 3E: Read Switch Status Register

The Read Switch Status register presents the state of each input and is a read-only register. Once the next command is sent, all of the inputs (SG/SP) are provided as a return. Logic '1' indicates that the corresponding switch is closed, while logic '0' means the switch is open.

Two additional bits are included in the status register, namely the Fault Status bit and the INTflg bit. The Fault Status bit is formed by combining the extended status bits and the wetting current fault bits. If any of these constituent bits are set, then the Fault Status bit will also be set. The INTflg bit is set whenever an interrupt happens on this device.

After POR, both the Fault Status bit and the INTflg bit are set to high to signify that an interrupt has occurred due to the POR event. The INTflg bit will be cleared when the Read Switch Status register is read. However, the Fault Status bit will stay high until the Fault Status register is read, at which point the POR fault bit and all other fault flags are cleared.

The Fault Status and INTflg bits are considered semi-global flags. In the event that a fault or an interrupt takes place, these bits will be returned after any command is written or read, with the exception of the SPI check and the Wetting Current Configuration registers. These two specific registers use those bits to set or display the configuration of the device.

The device has a fault or switch status detection capability which includes one internal 24-bit register. See Register # 42: Fault Status Register for more details. Bits 0 to 21 indicate the status of each input, where logic '1' represents a closed switch and logic '0' represents an open switch. Besides the input status information, details regarding fault status like die over-temperature, Hash fault, SPI errors, as well as interrupts are also reported.

An SPI read cycle is started by a transition of the CS_B pin from logic '1' to '0'. Subsequently, 32 SCLK cycles are required to shift the contents of the Fault Status registers out through the MISO pin. The INT_B pin is cleared 1μs after the falling edge of CS_B. However, if the fault condition still persists, the fault is immediately set again. The Fault Status bit is set whenever a fault occurs, and in order to clear the Fault status flag, the fault register must be read.

The INTflg bit is set whenever an interrupt event takes place, such as a change in the state of a switch or when any fault status bit is set. Any SPI message that returns the INTflg bit will clear this flag, even if the event is still ongoing. For instance, in the case of an over-temperature situation, it will trigger an interrupt. Although the interrupt can be cleared, the chip will not generate another interrupt due to the over-temperature until that fault has disappeared.

SPI CONTROL REGISTER (continued)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R	0011 111	MISO Return Word: 0011 1110
D[24]	TYPE	R	0	
D[23]	FAULT STATUS	R	1	0 = No Fault 1 = A fault has occurred. View this fault in the fault status register.
D[22]	INTflg	R	1	0 = No Change of state. 1 = Change of state detected
D[21:14]	SP[7:0]	R	X	SP7 ~ SP0 Input Status. 0 = Open Switch 1 = Closed Switch
D[13:0]	SG[13:0]	R	X	SG13 ~ SG0 Input Status. 0 = Open Switch. 1 = Closed Switch.

Register # 42: Fault Status Register

This register is intended to acquire the fault information by sending the address of the fault status register and the user will receive the corresponding information after sending the next SPI command from the MISO return word.

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	R	0100 001	MISO Return Word: 0100 0010
D[24]	TYPE	R	0	
D[23]	RESERVED	R	0	Fault Status
D[22]	INTflg	R	X	It reports that an interrupt has occurred. Read the status register to determine the cause. Set: Various (SGx change of state, SPx change of state, Extended status bits). Reset: Clear of fault or read of status register.
D[21:11]	RESERVED	R	00 0000 0000 0	Reserved
D[10]	SPI Error	R	X	It reports SPI error has occurred, such as incorrect module, incorrect address. Set: SPI message error occurs. Reset: Read Fault Status register and no SPI errors are detected.
D[9]	Hash Fault	R	X	SPI register whether match the hash. Set: The SPI register does not match the hash. Reset: The SPI register matches the hash.
D[8]	RESERVED	R	0	Reserved
D[7]	UV	R	X	It reports that the V_{BATP} voltage is in under-voltage condition. Set: The V_{BATP} voltage drops below UVLO falling threshold. Reset: Under-voltage condition disappears and fault flag is read (SPI).
D[6]	OV	R	X	It reports that the V_{BATP} voltage is in over-voltage condition. Set: The V_{BATP} voltage rises above over-voltage rising threshold. Reset: Over-voltage condition disappears and fault flag is read (SPI).
D[5]	Temp Flag	R	X	Temperature warning event has occurred. Set: The IC temperature exceeds thermal warning threshold T_{FLAG}. Reset: The IC temperature drops below T_{FLAG} - T_{LIM_HYS}, and fault flag is read (SPI).
D[4]	OT	R	X	Over-temperature event has occurred. Set: The IC temperature exceeds thermal limit T_{LIM}. Reset: The IC temperature drops below T_{LIM} - T_{LIM_HYS}, and fault flag is read (SPI).
D[3]	INT_B Wake	R	X	The external INT_B falling edge can wake the IC from the LPM. Set: The external INT_B falling edge wakes the IC from the LPM. Reset: SPI flag read.
D[2]	WAKE_B Wake	R	X	The external WAKE_B falling edge can wake the IC from the LPM. Set: The external WAKE_B falling edge wakes the IC from the LPM. Reset: SPI flag read.
D[1]	SPI Wake	R	X	A SPI message can wake the IC from the LPM. Set: An SPI message wakes the IC from the LPM. Reset: Flag read (SPI).
D[0]	POR	R	X	It reports a POR event has occurred. Set: The VBATP voltage drops below power-on reset voltage. Reset: Flag read (SPI).

SPI CONTROL REGISTER (continued)

Register # 47: Interrupt Request Register

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	W	0100 011	MISO Return Word: 0100 0111
D[24]	TYPE	W	1	
D[23:0]	INTERRUPT	W	0x000000	This register is intended to send a pulse with 110μs duration (active low). Bit 23: Fault Status Bit 22: INTflg Note that only the interrupt request command will not put the INTflg bit to '1' unless a fault or switch state change takes place.

Register # 49: Reset Register

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[31:25]	ADDRESS	W	0100 100	MISO Return Word: 0011 1110
D[24]	TYPE	W	1	
D[23:0]	RESET	W	0x000000	This register is intended to reset all the registers. Bit 23: Fault Status Bit 22: INTflg

APPLICATION INFORMATION

Application Diagram

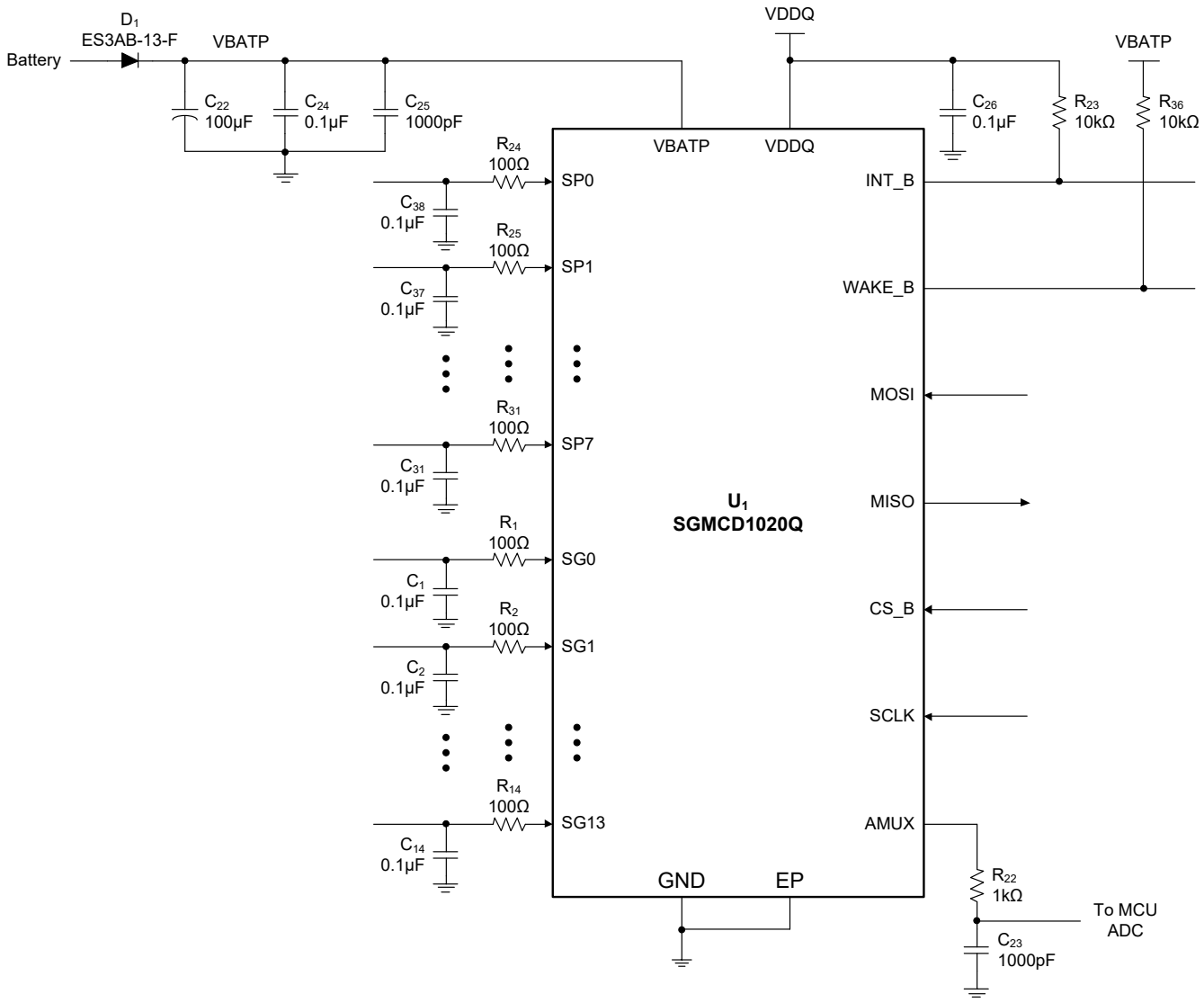


Figure 20. Typical Application Diagram

Bill of Materials

Table 2. Bill of Materials

Item	Quantity	Reference	Value	Description
1	24	C_1, ~ C_{14}, C_{24}, C_{26}, C_{31} ~ C_{38}	0.1μF	CAP CER 0.1μF 100V X7R 10% 0603
2	1	C_{22}	100μF	CAP ALEL 100μF 50V 20% – SMD
3	2	C_{23}, C_{25}	1000pF	CAP CER 1000pF 100V 10% X7R 0603
4	1	D_1	—	DIODE RECT 3.0A 50V AEC-Q101 SMB
5	22	R_1 ~R_{14}, R_{24} ~ R_{31}	100Ω	RES MF 100 0.5W 1% 0805
6	1	R_{22}	1.0kΩ	RES MF 1k 0.5W 5 % 0805
7	1	R_{23}	10kΩ	RES MF 10k 0.5W 5 % 0805 (optional)
8	1	R_{36}	10kΩ	RES MF 10k 0.5W 5 % 0805
9	1	U_1	SGMCD1020Q	IC Multiple Detection Switch Interface, TQFN-5×5-32GL

APPLICATION INFORMATION (continued)

Abnormal Operation

Seven abnormal cases of the SGMCD1020Q are provided for reference.

Reverse Battery

In reverse battery application, the SGMCD1020Q can handle negative voltage up to -14V for all SP/SG inputs. Hence, devices connecting to SGMCD1020Q are safely protected.

Ground Offset

The SGMCD1020Q is able to work normally under the ground offset application of up to ±1V. Note that the SP/SG voltage information transferred to the AMUX pin may varies due to the ground offset.

Shorts to Ground

The SGMCD1020Q is able to withstand -1V voltage with respect to the ground level when the SP/SG pins are shorted to GND.

Shorts to Battery

The SGMCD1020Q is able to withstand 40V voltage with respect to the ground level when the SP/SG pins are shorted to the battery. Though application depended, the voltage that SP/SG pins are shorted to may vary, but should be lower than 40V.

Unpowered Shorts to Battery

The SGMCD1020Q is able to withstand 40V voltage with respect to the ground level when the SP/SG pins are shorted to the battery that not connected with the SGMCD1020Q. In this case, no effective output is present and no backflow current to the VBATP, VDDQ or other SPI-related pins is witnessed.

Loss of Module Ground

When the ground of SGMCD1020Q is missed, all I/O pins are floating to the battery. For outside pins, they may bear the conditions of shorted to GND. Leakage current generated by loss of GND is limited by the SGMCD1020Q.

Loss of Module Battery

When the battery of SGMCD1020Q is missed, all I/O pins are floating to the ground. For outside pins, they should cope with leakage current flowing into the GND caused by external driver. Leakage current generated by loss of GND is limited by the SGMCD1020Q.

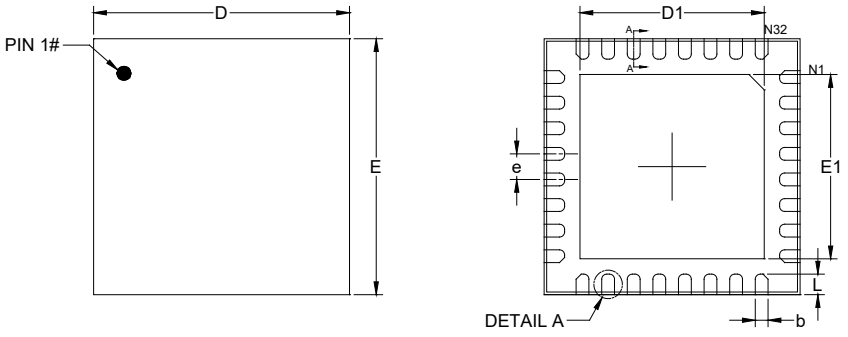
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

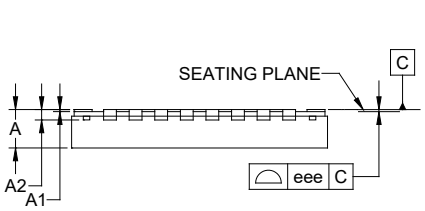
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

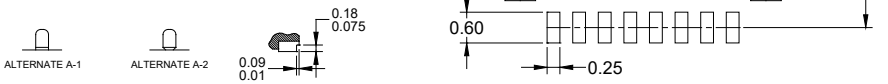
TQFN-5×5-32GL



TOP VIEW **BOTTOM VIEW**



SIDE VIEW



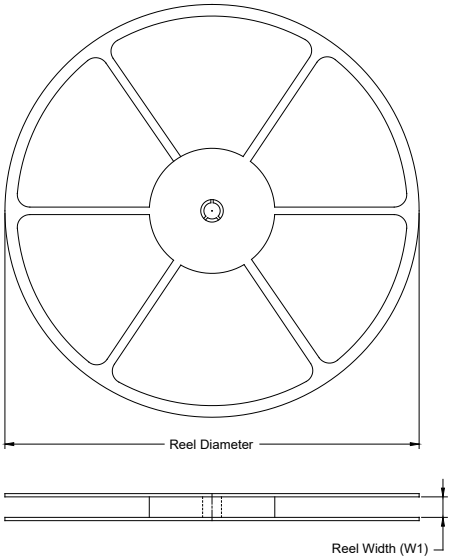
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.500	-	3.700
E1	3.500	-	3.700
e		0.500 BSC	
L	0.300	-	0.500
eee		0.080	

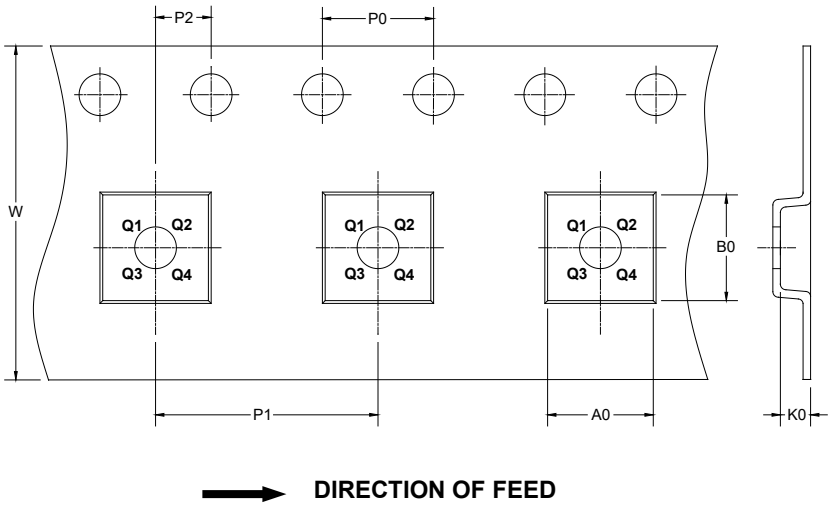
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



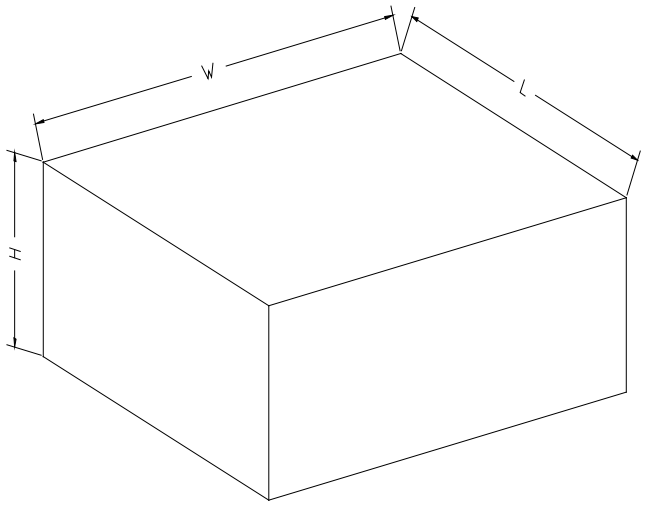
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32GL	13"	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002