SGM41298

1.5A Thermoelectric Cooler (TEC) Driver

GENERAL DESCRIPTION

The SGM41298 is a monolithic thermoelectric cooling (TEC) thermostat driver device with two-stage feedback amplifier. The device includes a differential driver (output) stage, an internal 2.5V output reference voltage and two zero-drift, rail-to-rail chopper amplifiers. The first chopper amplifier biases the sensed temperature signal and another is an error amplifier for compensating the closed loop temperature control. This amplifier can be used with a digital controller as well.

The TEC is driven differentially between a linear push-pull stage and a pulse-width modulation (PWM) switching stage. A linear push-pull stage forms one of the arms of the differential output which has a relatively high gain and saturates if the error signal is not close to zero (> 2.5%). This means that the TEC is effectively driven by the other arm. The other arm has a lower gain, and high frequency PWM switching driver that can drive the TEC with high efficiency. The PWM switching driver output is passed through an LC filter to remove large voltage ripple before reaching the TEC. It can sink or source current for both the heating and cooling modes connected to the TEC and stabilize its temperature at the set point.

The SGM41298 is available in a Green WLCSP-2.55×2.55-25B package. It operates over the -40℃ to +125℃ junction temperature range.

FEATURES

- **High Efficiency Single Inductor Architecture**
- **Single-ended to Differential Driver with Low R_{DSON} MOSFETs inside**
- **TEC Voltage and Current Monitoring**
- **No External Sense Resistor Required**
- **Independent Heating and Cooling Current/Voltage Limits Programming**
- **PWM Driver Switching Frequency: 2.0MHz (TYP)**
- **Two Rail-to-Rail, Zero-Drift Chopper Amplifiers**
- **Compatible with RTD or NTC Thermal Sensors**
- **2.5V Output Reference Voltage**
- **Patent Pending**
- **Available in a Green WLCSP-2.55×2.55-25B Package**

APPLICATIONS

TEC Temperature Controls
Instruments Requiring TEC Temperature Controls
Optical Modules
Optical Fiber Amplifiers
Optical Networking Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41298	WLCSP-2.55×2.55-25B	-40℃ to +125℃	SGM41298XG/TR	SGM 41298XG XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

PVIN to PGNDL .... -0.3V to 6V
PVIN to PGNDS.. -0.3V to 6V
LDR to PGNDL ....-0.3V to V_{PVIN}
SW to PGNDS .... -0.3V to 6V
AGND to PGNDL .... -0.3V to 0.3V
AGND to PGNDS.. -0.3V to 0.3V
VREF, SFB, VLIM_nSD, ILIM, IN1P, IN1N, IN2P, IN2N and EN to AGND ....-0.3V to V_{DD} + 0.3V
VDD, OUT1, OUT2, ITEC and VTEC to AGND ... -0.3V to 6V
Maximum Current
VREF to AGND..20mA
OUT1, OUT2, ITEC and VTEC to AGND......................50mA
Package Thermal Resistance
WLCSP-2.55×2.55-25B, θ_{JA} .... 53℃/W
Junction Temperature..+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility
HBM...4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Driver Supply Voltage Range..............................2.7V to 5.5V
Controller Supply Voltage Range........................2.7V to 5.5V
Operating Ambient Temperature Range......-40℃ to +125℃
Operating Junction Temperature Range......-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

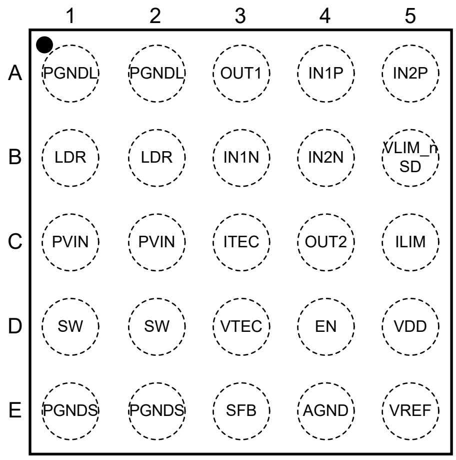
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.55×2.55-25B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1, A2	PGNDL	Power Ground of the Linear Driver Arm.
A3	OUT1	Output of the A1 Amplifier.
A4	IN1P	Non-Inverting Input of the A1 Amplifier.
A5	IN2P	Non-Inverting Input of the A2 (Compensation) Amplifier.
B1, B2	LDR	Output of the Linear Driver Arm.
B3	IN1N	Inverting Input of the A1 Amplifier.
B4	IN2N	Inverting Input of the A2 (Compensation) Amplifier.
B5	VLIM_nSD	Voltage Limit/Shutdown Input. This pin sets the cooling and heating TEC voltage limits (positive or negative TEC voltage limit). The device shuts down when it is pulled low.
C1, C2	PVIN	Power Supply Input for the TEC Controller.
C3	ITEC	TEC Current Monitoring Output.
C4	OUT2	Output of the A2 (Compensation) Amplifier.
C5	ILIM	Current Limit Setting Input. This pin sets the heating current limits and TEC cooling.
D1, D2	SW	Switch Node Output of the PWM Driver Arm.
D3	VTEC	TEC Voltage Monitoring Output.
D4	EN	Enable. Should be set high to enable the device.
D5	VDD	Power Input for the Device.
E1, E2	PGNDS	Power Ground of the PWM Driver Arm.
E3	SFB	Feedback Input of the PWM TEC Driver Output Voltage (After LC Filter).
E4	AGND	Signal Ground.
E5	VREF	2.5V Reference Output.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V to 5.5V, T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Driver Supply Voltage	V_{PVIN}		2.7		5.5	V
Controller Supply Voltage	V_{DD}		2.7		5.5	V
V_{DD} Over-Voltage Protection Threshold	V_{OVP}		5.56	5.75	5.95	V
OVP Hysteresis			5	35	60	mV
Supply Current	I_{DD}	PWM not switching		1.3	2	mA
Shutdown Current	I_{SD}	EN = AGND or VLIM_nSD = AGND		200	350	μA
Under-Voltage Lockout (UVLO)	V_{UVLO}	V_{DD} rising	2.50	2.58	2.66	V
UVLO Hysteresis	V_{UVLO_HYST}			90		mV
Reference Voltage	V_{REF}	I_{REF} = 0mA to 10mA	2.475	2.500	2.525	V
Linear Output						
Low Output Voltage	V_{LDR}	I_{LDR} = 0A		0		V
High Output Voltage				V_{PVIN}		V
Maximum Source Current	I_{LDR_SOURCE}		1.5			A
Maximum Sink Current	I_{LDR_SINK}				1.5	A
P-MOSFET On-Resistance	$R_{DS\_PL(ON)}$	I_{LDR} = 1.5A, V_{PVIN} = 5.0V		32	60	mΩ
		I_{LDR} = 1.5A, V_{PVIN} = 3.3V		40	70	
N-MOSFET On-Resistance	$R_{DS\_NL(ON)}$	I_{LDR} = 1.5A, V_{PVIN} = 5.0V		23	60	mΩ
		I_{LDR} = 1.5A, V_{PVIN} = 3.3V		28	70	
P-MOSFET Leakage Current	$I_{LDR\_P\_LKG}$			0.1	5	μA
N-MOSFET Leakage Current	$I_{LDR\_N\_LKG}$			100	180	μA
Linear Amplifier Gain	A_{LDR}			40		V/V
LDR Short-Circuit Threshold	$I_{LDR\_SH\_GNDL}$	LDR short to PGNDL, enter hiccup		4.5		A
	$I_{LDR\_SH\_PVIN}$	LDR short to PVIN, enter hiccup		-4.5		A
Hiccup Cycle	t_{HICCUP}			15		ms
PWM Output						
Low Output Voltage	V_{SFB}	I_{SFB} = 0A		0.06 × V_{PVIN}		V
High Output Voltage		I_{SFB} = 0A		0.93 × V_{PVIN}		V
Maximum Source Current	I_{SW_SOURCE}		1.5			A
Maximum Sink Current	I_{SW_SINK}				1.5	A
P-MOSFET On-Resistance	$R_{DS\_PS(ON)}$	I_{SW} = 1.5A, V_{PVIN} = 5.0V		31	60	mΩ
		I_{SW} = 1.5A, V_{PVIN} = 3.3V		38	70	
N-MOSFET On-Resistance	$R_{DS\_NS(ON)}$	I_{SW} = 1.5A, V_{PVIN} = 5.0V		20	50	mΩ
		I_{SW} = 1.5A, V_{PVIN} = 3.3V		25	60	
P-MOSFET Leakage Current	$I_{SW\_P\_LKG}$			0.1	5	μA
N-MOSFET Leakage Current	$I_{SW\_N\_LKG}$			0.1	5	μA
PWM Duty Cycle	D_{SW}	The range that continuous PWM operation is kept.	6		93	%
SFB Input Bias Current	I_{SFB}			60	100	μA
Internal Oscillator Frequency	f_{OSC}	EN high	1.76	2.00	2.24	MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 5.5V, T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Low Input Voltage	V_{IL}				0.8	V
EN High Input Voltage	V_{IH}		2.1			V
EN Input Current	I_{EN}			0.3	1	μA
Pull-Down Current				0.3	2	μA
Error/Compensation Amplifiers						
Input Offset Voltage	V_{OS1}	V_{CM1} = 1.5V, V_{OS1} = V_{IN1P} - V_{IN1N}		10	100	μV
	V_{OS2}	V_{CM2} = 1.5V, V_{OS2} = V_{IN2P} - V_{IN2N}		10	140	μV
Input Voltage Range	V_{CM1}, V_{CM2}		0		V_{DD}	V
Common Mode Rejection Ratio	CMRR	V_{CM1}, V_{CM2} = 0.2V to V_{DD} - 0.2V		120		dB
High Output Voltage	V_{OH1}, V_{OH2}	I_{OUT1} = I_{OUT2} = 5mA	V_{DD} - 0.15			V
Low Output Voltage	V_{OL1}, V_{OL2}	I_{OUT1} = I_{OUT2} = 5mA			150	mV
Power Supply Rejection Ratio	PSRR			120		dB
Output Current	I_{OUT1}, I_{OUT2}	Sourcing and sinking	5			mA
Gain Bandwidth Product	GBW	V_{OUT1}, V_{OUT2} = 0.5V to V_{DD} - 1V		1		MHz
TEC Current Limit						
Current-Limit Threshold (Cooling)	V_{ILIMC_TH}	V_{ITEC} = 2V	1.98	2.0	2.02	V
Current-Limit Threshold (Heating)	V_{ILIMH_TH}	V_{ITEC} = 0.5V	0.48	0.50	0.52	V
ILIM Input Current (Cooling)	I_{ILIMC}	Sourcing current	37	40	43	μA
ILIM Input Current (Heating)	I_{ILIMH}			0.01	1	μA
Cooling to Heating Current Detection Threshold	$I_{COOL\_HEAT\_TH}$			40		mA
TEC Voltage Limit						
Voltage Limit Gain	A_{VLIM}	(V_{DRL} - V_{SFB})/V_{VLIM}		2		V/V
VLIM_nSD Input Current (Cooling)	I_{VLIMC}	V_{OUT2} < V_{REF}/2		0.1	1	μA
VLIM_nSD Input Current (Heating)	I_{VLIMH}	V_{OUT2} > V_{REF}/2, sinking current	8	10	12	μA
TEC Current Measurement						
Current Sense Gain	R_{CS}	V_{PVIN} = 3.3V		0.525		V/A
		V_{PVIN} = 5V		0.520		
Current Measurement Accuracy	I_{LDR_ERROR}	700mA ≤ I_{LDR} ≤ 1.5A, V_{PVIN} = 3.3V	-10		10	%
		800mA ≤ I_{LDR} ≤ 1.5A, V_{PVIN} = 5V	-12		12	
ITEC Voltage Accuracy	$V_{ITEC\_AT\_700\_mA}$	V_{PVIN} = 3.3V, cooling, V_{VREF}/2 + I_{LDR} × R_{CS}	1.570	1.625	1.680	V
	$V_{ITEC\_AT\_-700\_mA}$	V_{PVIN} = 3.3V, heating, V_{REF}/2 - I_{LDR} × R_{CS}	0.820	0.885	0.940	
	$V_{ITEC\_AT\_800\_mA}$	V_{PVIN} = 5V, cooling, V_{REF}/2 + I_{LDR} × R_{CS}	1.600	1.668	1.720	
	$V_{ITEC\_AT\_-800\_mA}$	V_{PVIN} = 5V, heating, V_{REF}/2 - I_{LDR} × R_{CS}	0.760	0.828	0.880	
ITEC Bias Voltage	V_{ITEC_B}	I_{LDR} = 0A	1.210	1.250	1.285	V
Maximum ITEC Output Current	I_{ITEC}		-2		2	mA

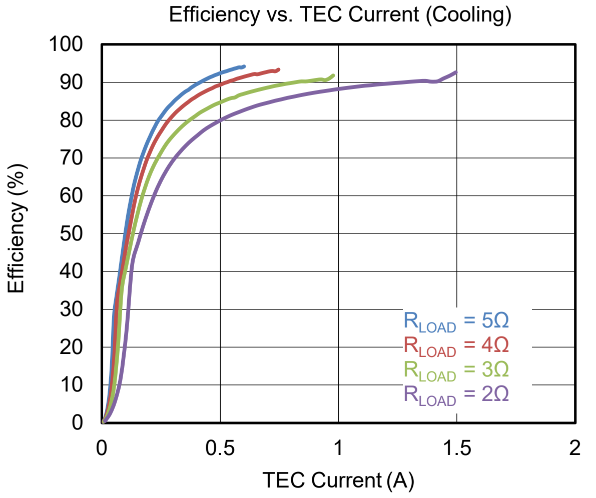
ELECTRICAL CHARACTERISTICS (continued)

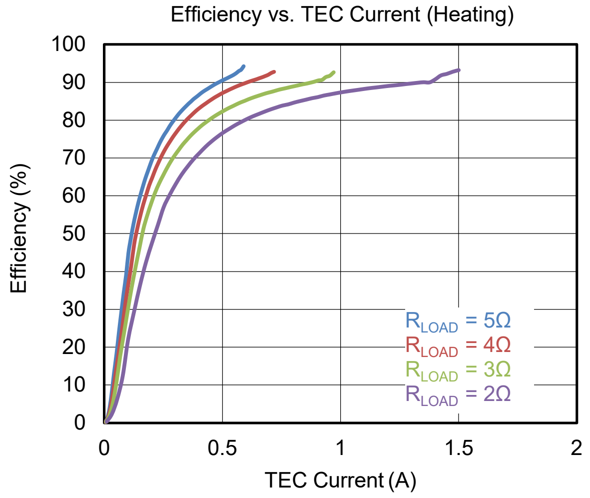
(V_{IN} = 2.7V to 5.5V, T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, unless otherwise noted.)

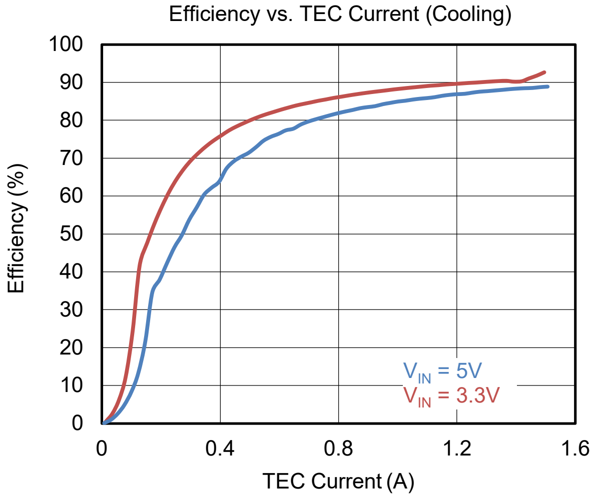
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEC Voltage Measurement						
Voltage Sense Gain	A_{VTEC}		0.24	0.25	0.26	V/V
Voltage Measurement Accuracy	$V_{VTEC\_AT\_1\_V}$	V_{LDR} - V_{SFB} = 1V, V_{REF}/2 + A_{VTEC} × (V_{LDR} - V_{SFB})	1.475	1.500	1.525	V
VTEC Bias Voltage	V_{VTEC_B}	V_{LDR} = V_{SFB}	1.225	1.250	1.285	V
Maximum VTEC Output Current	R_{VTEC}		-2		2	mA
Internal Soft-Start						
Soft-Start Time	t_{SS}			110		ms
VLIM_nSD Shutdown						
Low Voltage Threshold	$V_{VLIM\_nSD\_THL}$				0.07	V
Thermal Shutdown						
Threshold	T_{SHDN_TH}			170		°C
Hysteresis	T_{SHDN_HYS}			5		°C

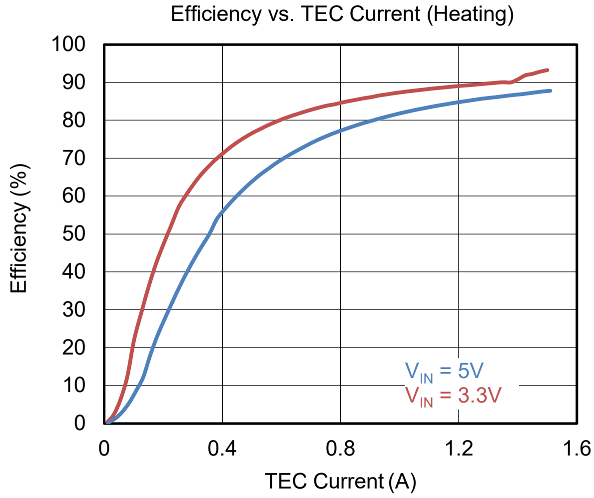
TYPICAL PERFORMANCE CHARACTERISTICS

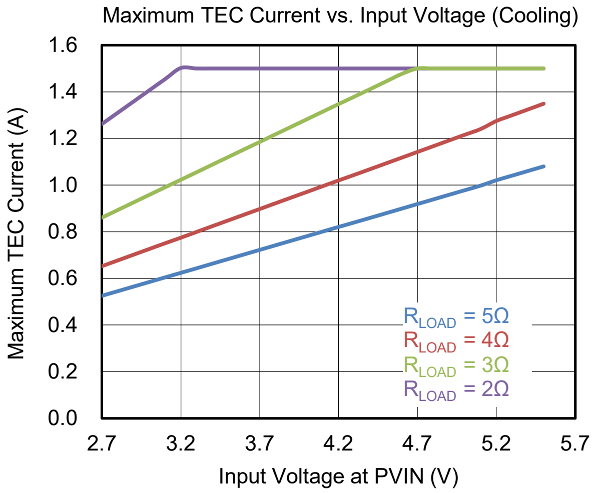
T_J = +25℃, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.

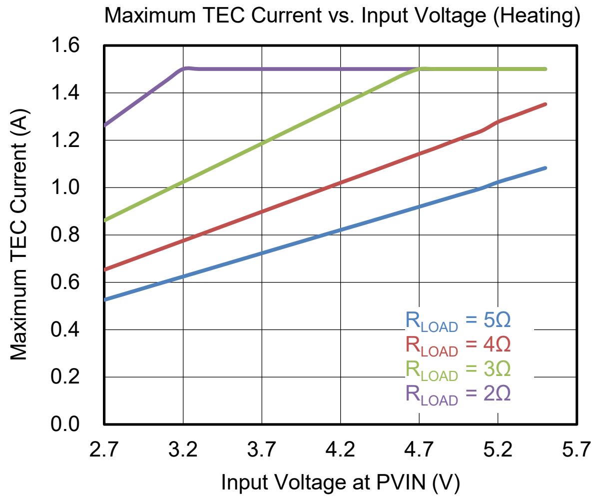








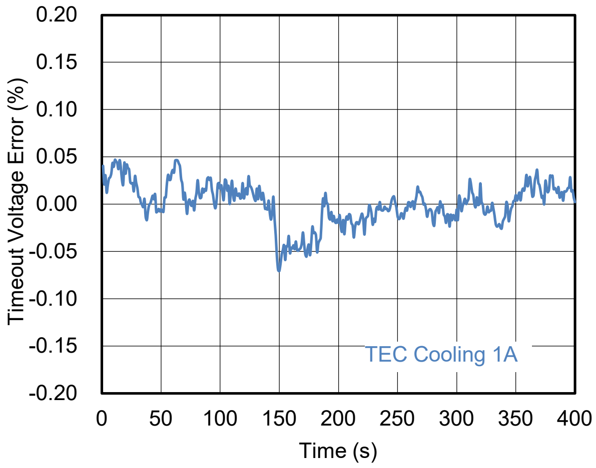




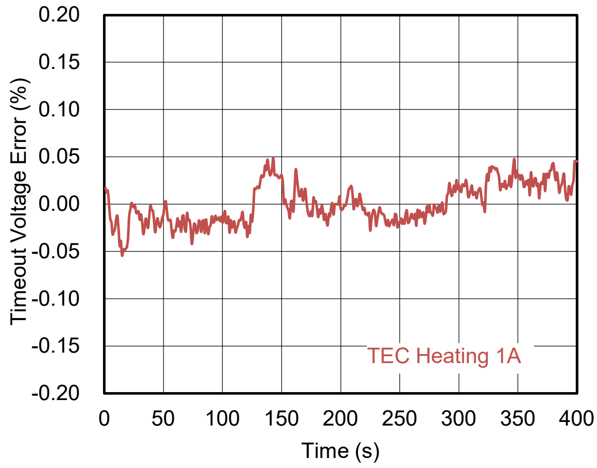
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.

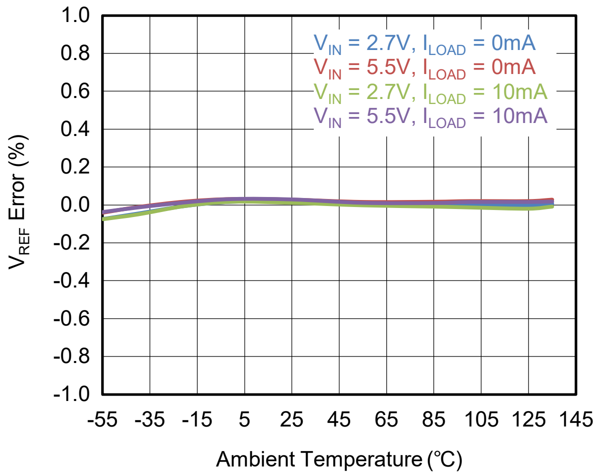
Differential Output Total Interference



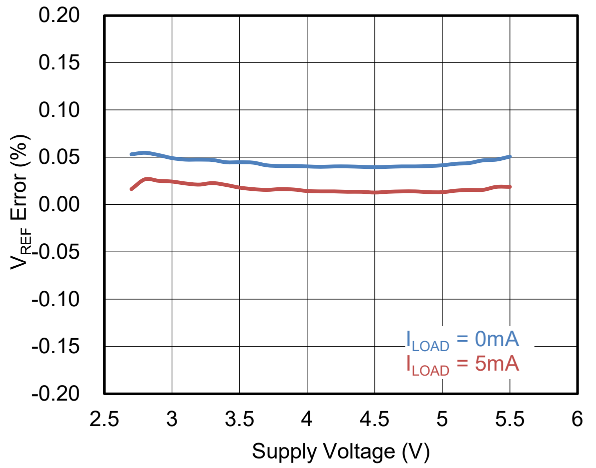
Differential Output Total Interference



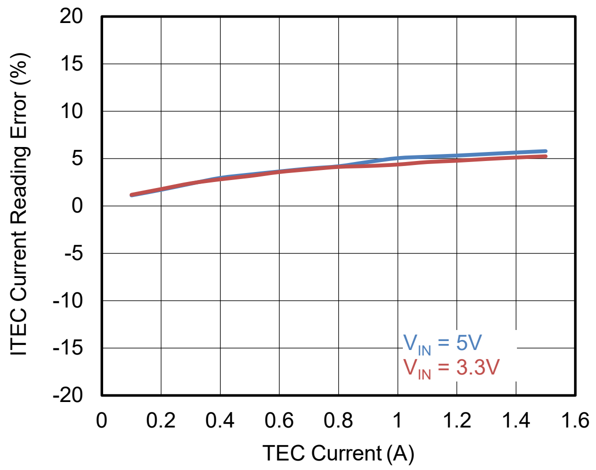
V_{REF} Error vs. Ambient Temperature



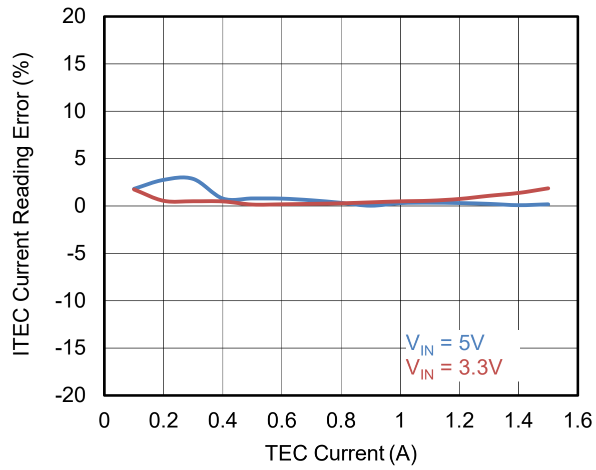
V_{REF} Line Regulation



ITEC Current Reading Error vs. TEC Current in Cooling Mode

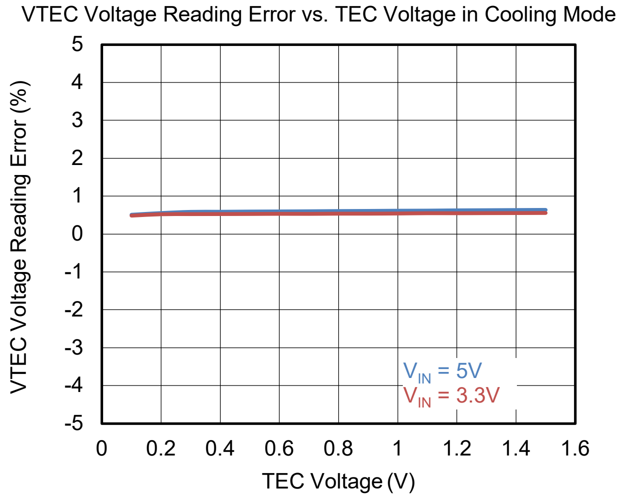


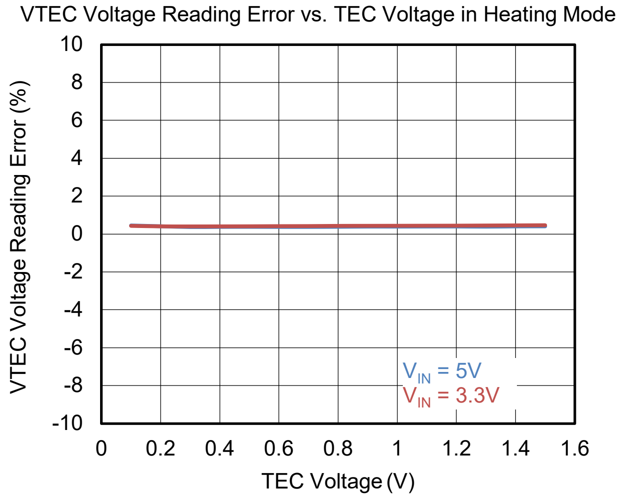
ITEC Current Reading Error vs. TEC Current in Heating Mode

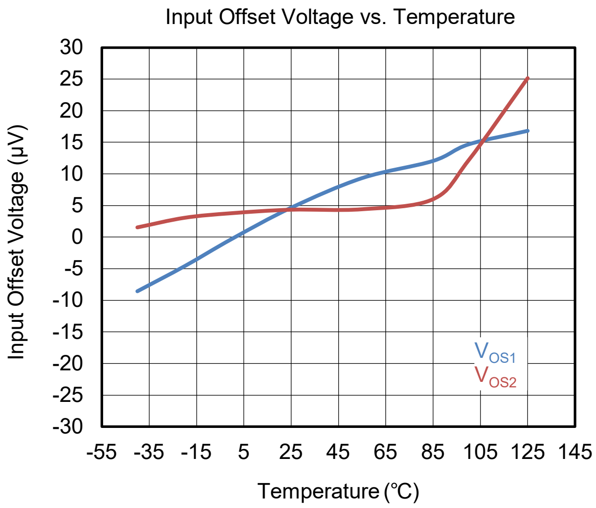


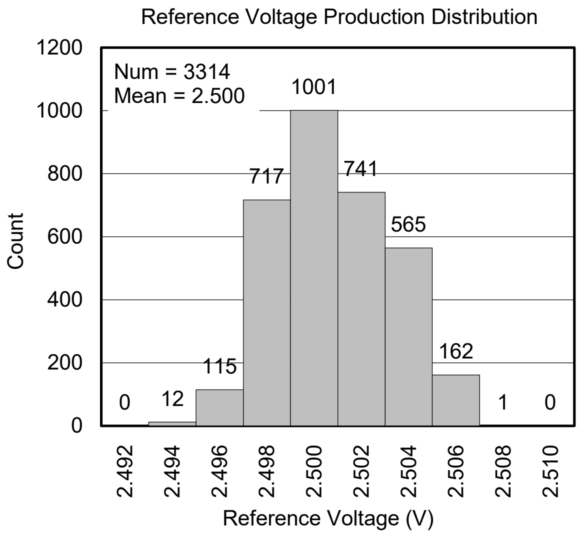
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.





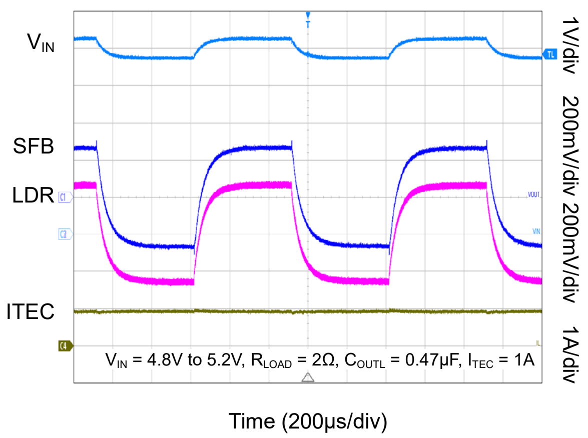




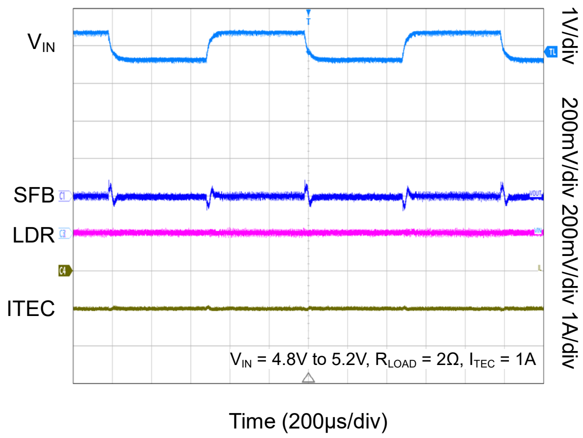
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25°C, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.

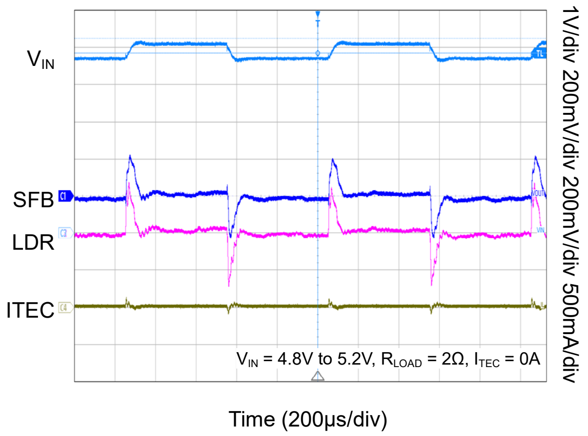
Line Transient in Cooling Mode



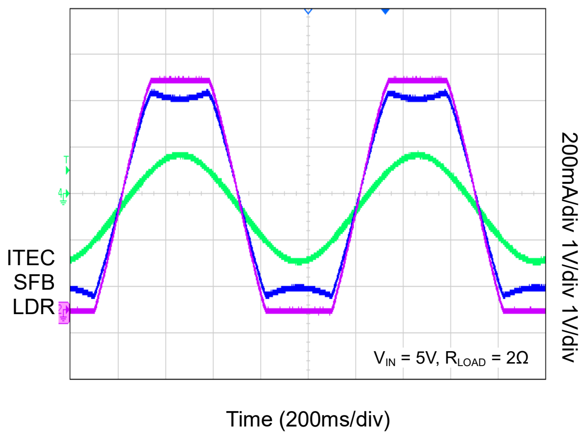
Line Transient in Heating Mode



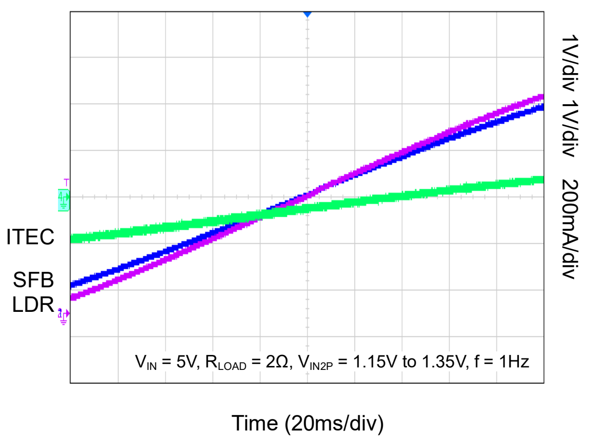
Line Transient



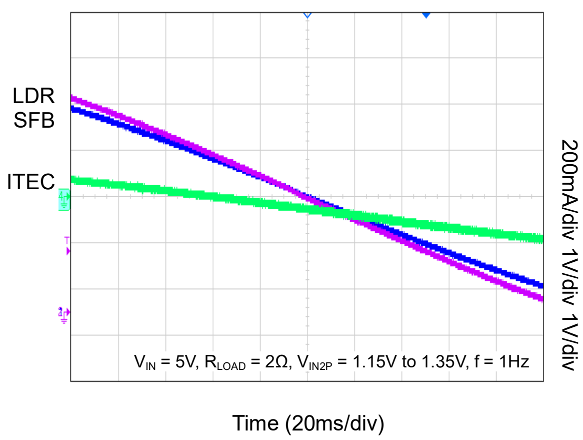
Cooling to Heating Transition



Zero-Crossing TEC Current Zoom In from Heating to Cooling



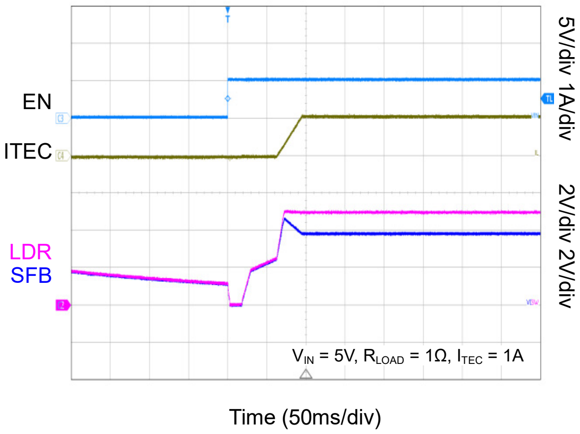
Zero-Crossing TEC Current Zoom In from Cooling to Heating



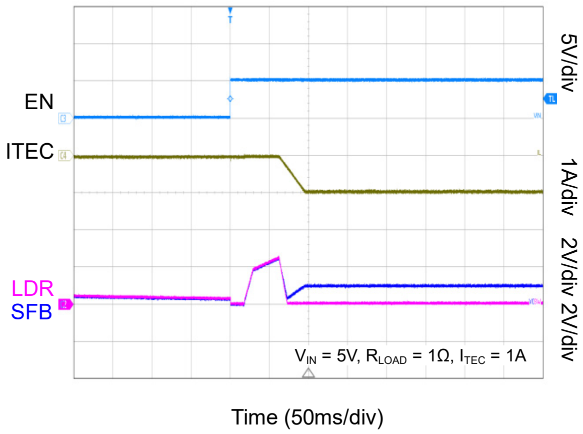
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.

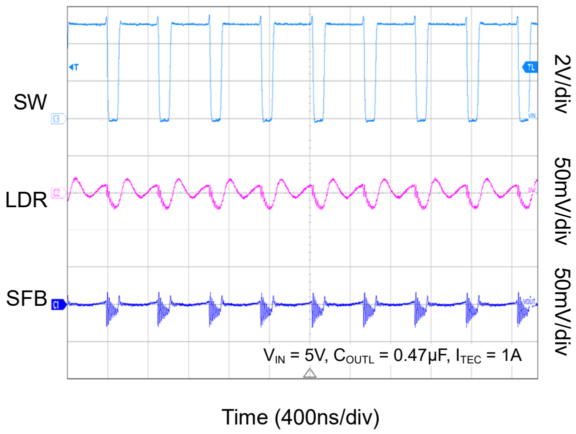
Typical Enable Waveforms in Cooling Mode



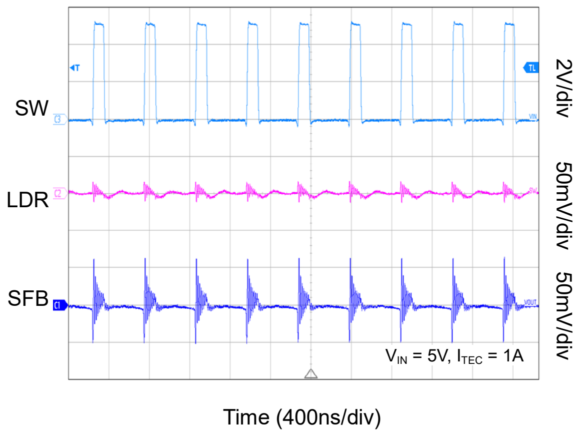
Typical Enable Waveforms in Heating Mode



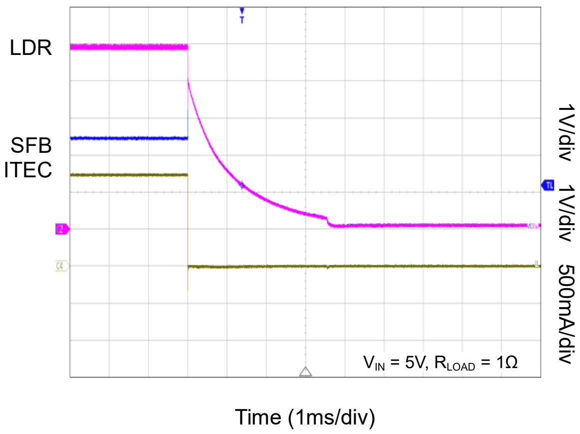
Typical Switch and Voltage Ripple Waveforms in Cooling Mode



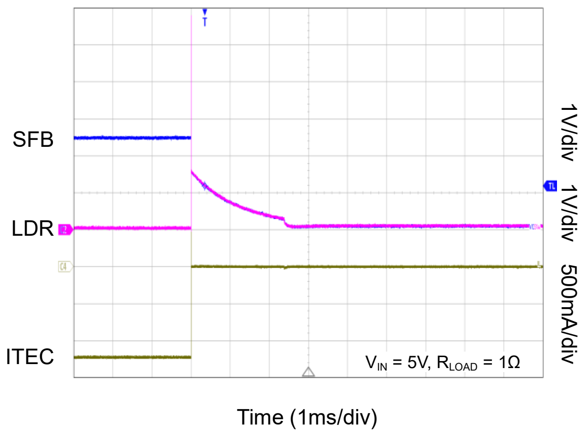
Typical Switch and Voltage Ripple Waveforms in Heating Mode



TEC Short in Cooling Mode



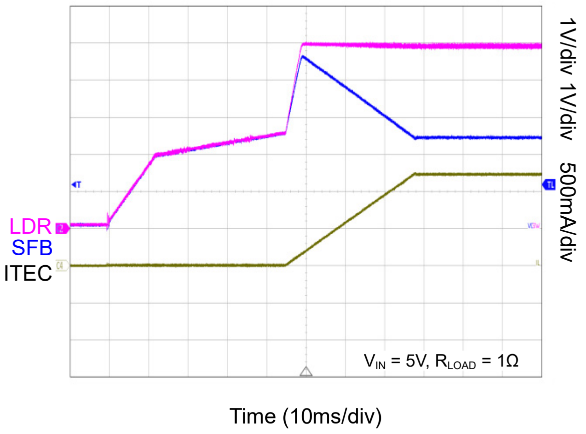
TEC Short in Heating Mode



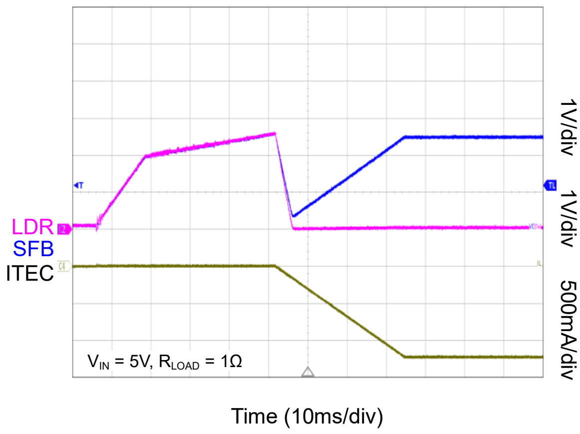
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{OUTS} = 10μF, C_{INS} = 10μF and L = 1μH, unless otherwise noted.

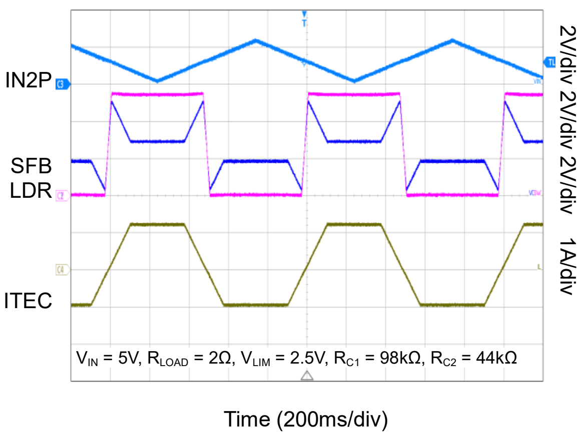
Recover from TEC Short in Cooling Mode



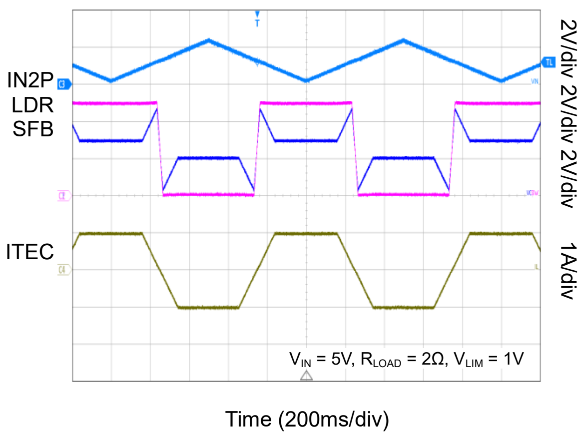
Recover from TEC Short in Heating Mode



Current Limit Response



Voltage Limit Response



FUNCTIONAL BLOCK DIAGRAM

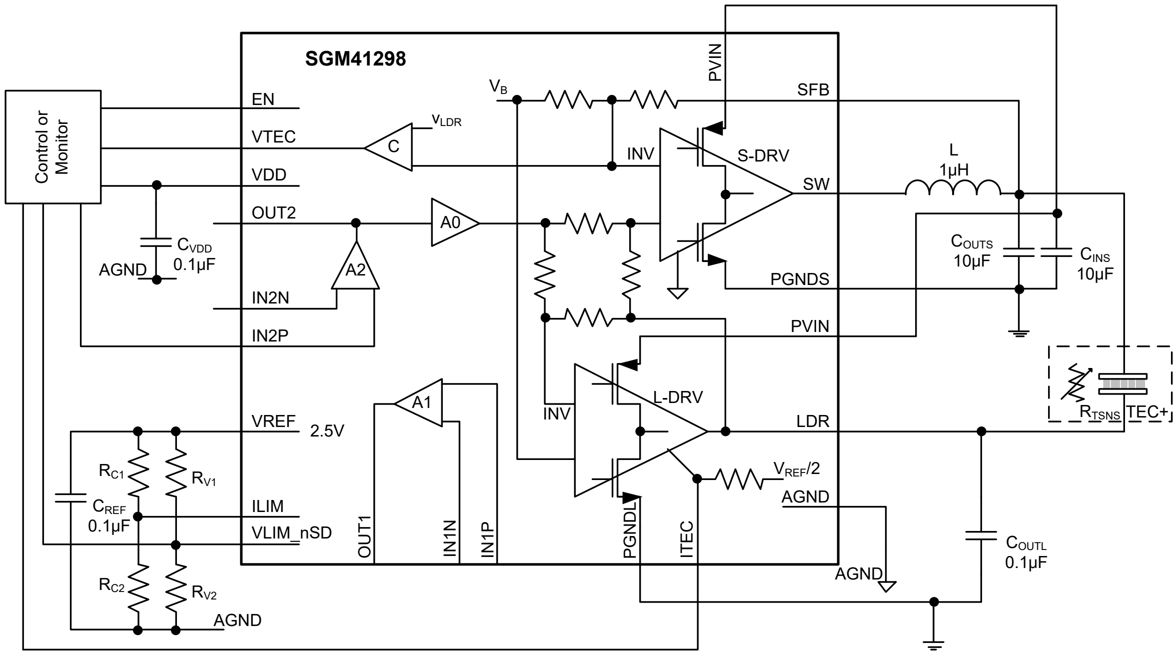


Figure 1. Block Diagram

OPERATION PRINCIPLE AND APPLICATION

The SGM41298 contains all the necessary circuits to make a full analog control loop for a TEC thermostat, including precision chopper amplifiers, TEC differential driver and reference voltage plus monitoring and limiting functions and protections for over-temperature and over-current (see Figure 1).

The differential driver has two arms: a linear arm with high transfer gain and a switching regulator arm with a relatively lower gain. With this structure, the precise but inefficient linear driver saturates at low differential output swing such that in most of the output range only the switching arm is effectively regulating the output. This keeps the overall driving efficiency very high and close to a common switching converter rather than a linear amplifier.

Figure 2 shows a model for the differential driver. The $V_{REF}/2$ = 1.25V is the common mode signal reference (zero) for the amplifiers. From the A0 input which is OUT2 from the compensator to the LDR output, the transfer ratio (V_{OUT2} -1.25 to V_{LDR} - V_B) is designed to be a 40× gain. The switching arm is designed to amplify the divider output (1/5 of the V_{LDR} - V_B) by 5× and 5/6 of V_{OUT2} - 1.25 by 6× gain. Overall, it makes the differential output to follow 5 × (V_{OUT2} - 1.25). Refer to the transfer plots in the typical performance characteristics for details.

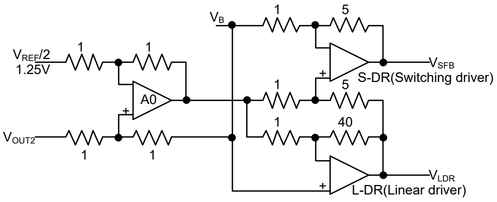


Figure 2. The Single-ended V_{OUT2} to Differential Output Transfer Model

The output current and voltage limits are independently set with programming resistor dividers (powered from V_{REF}) for both driving directions (sink and source). The bias currents can be different in each direction. This programming flexibility allows the operation range to be set for a wide range of TEC specifications.

Soft-Start

When the device starts to operate or resumes from the over-temperature or switch over-current protection conditions, both arms (the LDR and switching) output initially go to 0V and then ramp up to the common voltage of V_B (no differential driving at this moment) and then they start to split and the differential driving starts. Refer to the waveform captures in the typical performance characteristics for details. Before the differential outputs raise off the ground level enough, the internal cooling/heating current detection is not certain and the internal bias currents to VLIM and ILIM may toggle correspondingly.

Over-Voltage Protection

SGM41298 has an input over-voltage protection (OVP) to protect the device. When the V_{DD} voltage of the SGM41298 exceeds the OVP threshold of 5.75V, the device stops switching.

TEC Thermostat Basis

The TEC device is made of semiconductor (Bi_2Te_3) thermo-electric piles that have positive or negative mobility potentials in the P-doping or N-doping, in which the mobile charge is hotter or cooler than the bulk. When foreign chargers compensate the chargers of hot or cool spots, mobile chargers are released in even hotter or cooler spots and the procedure makes the bulk hotter or cooler.

Figure 3 shows the Voltage-Current (I-V) plots of a typical 9-coupler TEC sample at different thermal power transfer values when acting as a cooler. Derived from this figure, the thermal pumping efficiency is given in Figure 4 and the resistive loss to the leakage loss relationship is extracted and given in Figure 5. The Q = 0 curve shows the I-V points with the largest generated ΔT across TEC. The ΔT = 0 curve gives the I-V points with the highest heat transfer (thermal flux). The peak trace shows the maximum achievable ΔT for different thermal loads (heat transfer). After the peak trace and at higher currents the driver voltage to ΔT gain polarity is reversed so the cooling current must be carefully limited below the peak trace to maintain a monotonic relation between drive current and generated ΔT. This is essential for the stability and loop convergent.

OPERATION PRINCIPLE AND APPLICATION (continued)

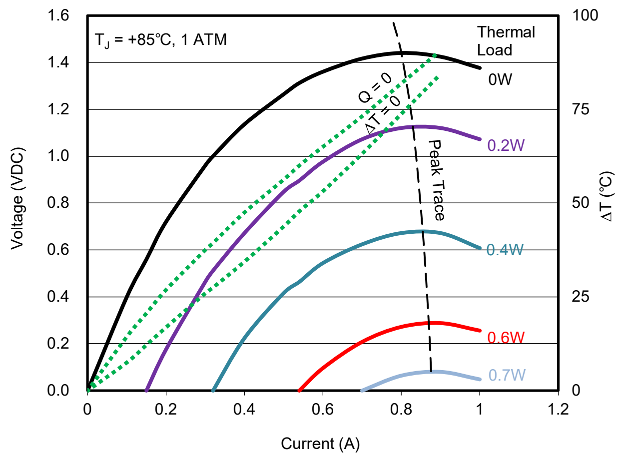


Figure 3. The Typical I-V and Thermal Transfer Plot

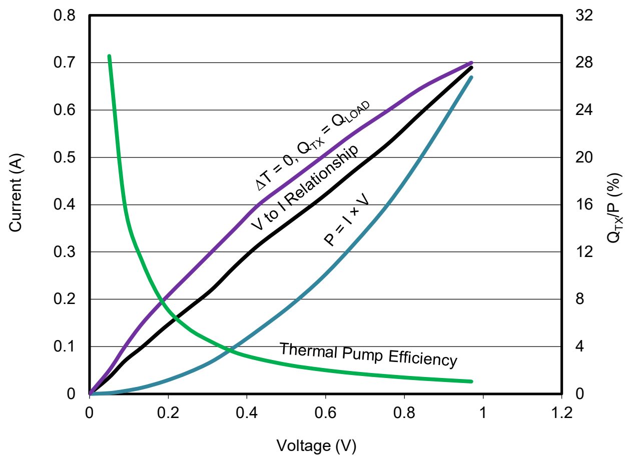


Figure 4. Thermal Pump Efficiency. The Q_{TX}/P is the Ratio of Transferred Heat to the Driving Power (in %)

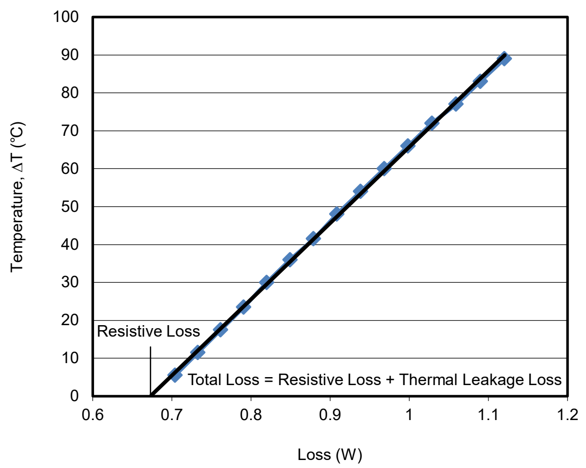


Figure 5. Resistive Loss and Thermal Leakage

From Figure 4 it can be concluded that a larger capacity TEC (capable for higher heat power transfer) has a better efficiency at the same heat load. Figure 5 illustrates that the TEC resistive loss (P = V × I) is bigger than leakage loss that is due to the natural heat transfer (leakage) through the thermal resistance of the TEC from the hot side to the cool side. The resistive loss is the dominant portion of the total loss.

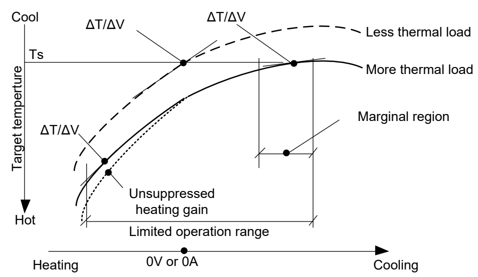


Figure 6. The Maximum and Suitable (below Marginal) Operating Ranges

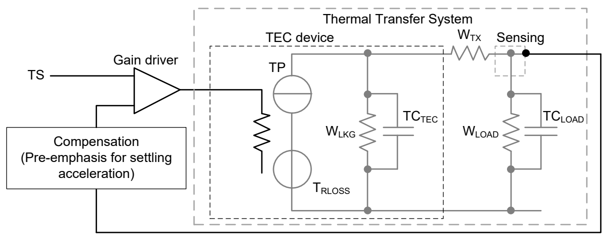


Figure 7. TEC Thermostat Combined Loop Model

Figure 6 shows that the ΔT/ΔV (differential gain of drive voltage to temperature difference) varies in the operation range and is smaller at higher thermal loads.

Figure 7 shows the closed loop model of a TEC thermostat with its dual major poles and other key elements in the thermal system. The load thermal capacitance TC_{LOAD} (heat capacity) and the heat transfer loss W_{TX} along with the TEC thermal capacitance (TC_{TEC}) results in a 2^{nd} order system for control loop to compensate. The TP stands for power of the thermal pump and T_{RLOSS} models the thermal leakage loss.

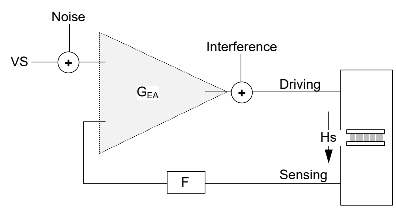


Figure 8. Error Sources in a TEC Thermostat

OPERATION PRINCIPLE AND APPLICATION (continued)

Based on the system model shown in Figure 8, if the temperature set point is VS, the deterministic temperature error T_{DE} and the sensed temperature T_{SNS} can be represented as:

$$T_{DE} = \frac{Noise}{F} + \frac{Hs}{1 + F \times Hs \times G_{EA}} \times Interference \quad (1)$$

$$T_{SNS} = \frac{VS}{F} \times \frac{G_{EA} \times Hs}{1 + G_{EA} \times Hs \times F} + T_{DE} \quad (2)$$

For the total interference value of the device, please refer to the SGM41298 typical performance characteristics table.

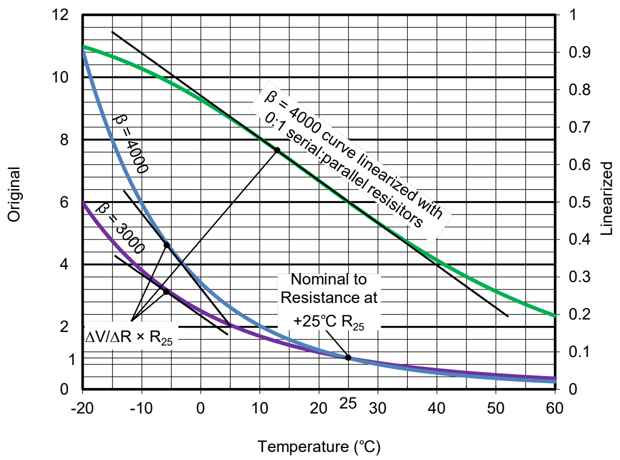


Figure 9. Typical NTC Responsivity and Linearization

TEC Thermostat Design

Several types of temperature sensors such as NTC, thermo-resistance (PTR), PN junction and thermocouples [1] can be used for sensing the temperature of the object to make a thermostat. The NTC without linearization has typically the largest responsivity in the cooling range and is suitable for TEC applications in the cooling mode.

For example, a typical PN junction type sensor has a responsivity of about -2mV/℃. A 1kΩ NTC with β = 3000 and 200μA bias has almost the same responsivity at 60℃. Such responsivity is good enough for most of the thermostat applications; the main design constrain is usually the transfer gain of the TEC device. The sensor system noise, settling time and system pull-in time are the 3 main challenges for a stable design. The thermal system noise impact can be mitigated by using a low noise sensor, using a stable driver or by increasing the load thermal capacity. The response time of a thermal system can also be improved by a pre-emphasizer stage. A digital PID compensator with the adaptive gain can be used instead of the analog one. This is better for design flexibility as it can easily fit different conditions.

Fast pull-in time is desired for quick calibration in production or for a quick set-up in a specific application. An error-adaptive gain (more gain when error is large and less gain when it is small) helps getting a calibration-free and fast pull-in performance for the loop. Having a digital segmented loop that has different loop gains for different error amplitude is more convenient for flexible parameter programming and achieving larger time constants.

Table 1. Factors to Consider in TEC Thermostat Design

Items	Description
Ambient Temperature	Design objective. The maximum temperature at which the thermostat can work.
Thermal Load	Design objective. The load and its transient condition, i.e., the power of the thermal load and how fast the load power changes in operation.
Control Range	Design objective. The temperature to maintain and its accuracy, resolution and its range.
Response Time	Design objective. The response time when the system is locked-in with limited ambient temperature interference sudden change.
Pull-In Time	Design objective. The time to pull the system in the locked-in status from the uncontrolled (loss of control) status during start-up or after pull-off by a heavy interference.
TEC Performance	Constrain condition verification. To evaluate or select a TEC device for its maximum cooling gain (at the highest available control temperature and maximum thermal load) and heating gain (at the lowest available control temperature and lowest thermal load).
Sensor Performance	Constrain condition verification, i.e., its worst responsivity in desired range. The key element affecting the thermostat performance.
Thermal Bias	Ambient impact, i.e., the bias power in the given ambient temperature range: TEC/object to ambient thermal coupling, a constrain condition for characterize in system.
Driving Response	The system characterization. The cooling gain and heating gain at segmented different TEC loading condition.
Injection Response	The system characterization, on both the thermal load injection response and thermal bias (ambient) injection.
System Noise	The actual/simulated system characterization.
Loop Gain/ Bandwidth	Design synthesis, derived from the objectives and conditions, matches with the sensor performance.
Loop Noise	Design synthesis, derived from the objectives and conditions.
Control Mode	Design synthesis, derived from the objectives and conditions.

[1] NTC is negative temperature co-efficiency resistor; PTR is positive temperature co-efficiency resistor like platinum film; junction voltage is the PN junction forward voltage bias with a constant current. The junction voltage type and thermal coupling may be easier to fabricate for integration.

OPERATION PRINCIPLE AND APPLICATION (continued)

Programming the Limits

Both current limit and voltage limit are set by similar internal circuits. Current and voltage limit points are sent to an operational trans-impedance amplifier with current sinking and sourcing capability. If the limits are reached, the switching arm output magnitude is reduced or is cut off to prevent damages.

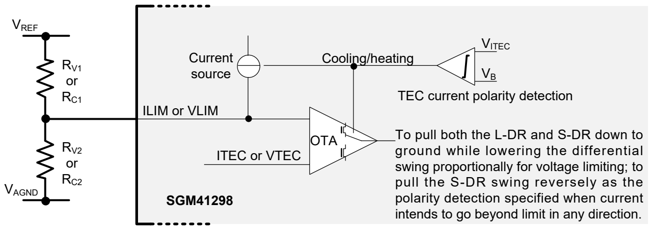


Figure 10. Voltage and Current Limit Circuit Architecture

As shown in Figure 10, the external resistor dividers (for voltage and current individually) for limit settings are biased with two current sinking/pouring sources. When the current polarity changes, the two bias current sources are turned on or off and injected into the resistor dividers, the voltages at VLIM or ILIM are set high or low to 1.25V, which is the corresponding value for both zero driving current and zero differential driving voltage. One bias current pours I_{ILIMC} (40μA) off the ILIM when driving is detected as in cooling direction and the other sinks I_{ILIMH} (10μA) into the VLIM when driving in heating direction. The 4 divider resistances are calculated from the following equations:

$$R_{V1} = 2.5 \times 10^5 \times \left(1 - \frac{V_{TEC\_MAX\_HEATING}}{V_{TEC\_MAX\_COOLING}}\right) \quad (3)$$

$$R_{V2} = R_{V1} \Big/ \left(\frac{5}{V_{TEC\_MAX\_COOLING}} - 1\right) \quad (4)$$

$$R_{C1} = 6.25 \times 10^4 \times \left(\frac{1.25 + 0.525 \times I_{TEC\_MAX\_COOLING}}{1.25 - 0.525 \times I_{TEC\_MAX\_HEATING}} - 1\right) \quad (5)$$

$$R_{C2} = R_{C1} \Big/ \left(\frac{2.5}{1.25 - 0.525 \times I_{TEC\_MAX\_HEATING}} - 1\right) \quad (6)$$

The $V_{TEC\_MAX\_HEATING}$, $V_{TEC\_MAX\_COOLING}$, $I_{TEC\_MAX\_HEATING}$ and $I_{TEC\_MAX\_COOLING}$ are parameters given for specific TEC device as listed maximum voltages and currents in its specification. The limiting voltage for either ILIM or VLIM in either cooling or heating should be far enough away from 1.25V, which is more than 50mV, to avoid unstable caused by impaired limiting direction when the setting current or voltage swing is too close to zero.

Output Monitoring and Reference Voltage

The differential output voltage and bidirectional output current are converted into single ended output signals (biased to $V_{REF}/2$ = 1.25V) for external monitoring (V_{TEC} and I_{TEC} output voltages). The characteristic parameters of these monitoring outputs and the reference voltage (V_{REF}, which is used for biasing external sensing networks) and the temperature-good signal are given in the SGM41298 electrical characteristics table.

Designing the Analog Loop

A1 is a chopper amplifier designed for temperature sensor signal conditioning (such as changing its polarity, adjusting the offset or increasing its sensitivity). The chopper amplifier A2 is designed for making an error amplifier that provides gain and compensation to either an external control input or to the output of the chopper amplifier A1.

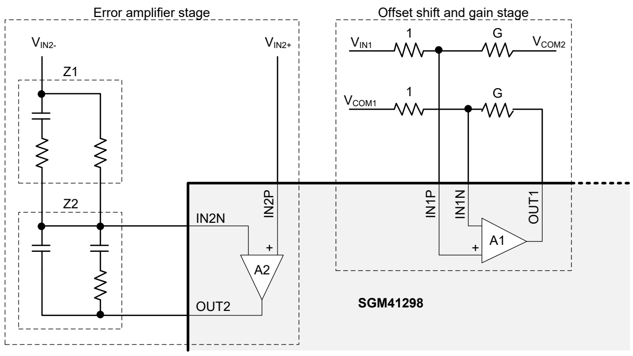


Figure 11. Using SGM41298 Amplifiers

Figure 11 shows an applicable circuit in which A2 is used to make an error amplifier with external compensation network Z1 and Z2, and A1 is used to make a gain (G) stage with level shifting from V_{COM1} at input side to V_{COM2} at output (OUT1). The temperature setting can be fed into either V_{IN2+} or V_{IN2-} and the temperature sensor (for example NTC) can replace one of the four resistors.

OPERATION PRINCIPLE AND APPLICATION (continued)

Operate as Driver in a Digital Loop

When the device is used in a digital thermostat loop, it works as a single-ended to differential power amplifier with programmable current limiting and voltage limiting. The single-ended input to the power stage is the OUT2 that is output of A2, which is centered to 1.25V and the differential swing is centered at 1.5V for V_{DD} < 4V or 2.5V for V_{DD} > 4V. The external input to the power amplifier should be applied through any of the amplifier input and then the A2 transfers to OUT2 for the power amplifier.

Either the voltage limiting or the current limiting is performed with a single amplifier for two directional limiting thresholds separately. The limiting directions and thresholds follow the change and match with the actual TEC driving polarity autonomously with the internal TEC current detection circuit. The mechanism of following has to be maintained is using DACs to programming the thresholds, which could be implemented by insertion of serial resistor between the DAC output to the VLIM or ILIM that enables the bias current changing the threshold matching the TEC driving polarity. Each threshold should sit aside 1.25V farer then 50mV minimally.

Layout and Component Selection

The PWM chopper and the L and C components need to be carefully placed and routed. Keep the key components (L, C_{INS}, C_{OUTS} and C_{OUTL}) close to the device and separate the high current and reference grounds and connect them in one point. Keep the switching current loop area as small as possible. Choose proper L, C_{INS}, C_{OUTS} and C_{OUTL} for operating frequency and currents and choose a low DCR inductor and low ESR capacitors.

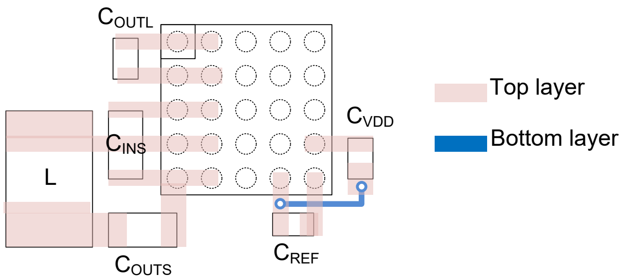


Figure 12. Key Components Placement and Layout

Table 2. Recommended Inductor and Capacitors

Designation	Vendor	Device No.	Value	Verified Suitable Range
L	Würth-Elektronik	74439344010	1μH	0.68μH ~ 1.5μH
C_{INS}	Murata	C426637/GRJ31CR71E106KE11L	10μF	≥ 10μF
C_{OUTS}	Murata	C426637/GRJ31CR71E106KE11L	10μF	10μF ~ 22μF
C_{OUTL}	Murata	0805B104K500NT	0.1μF	0.1μF ~ 1μF

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2022 – REV.A.2 to REV.A.3	Page
Updated Features section	1

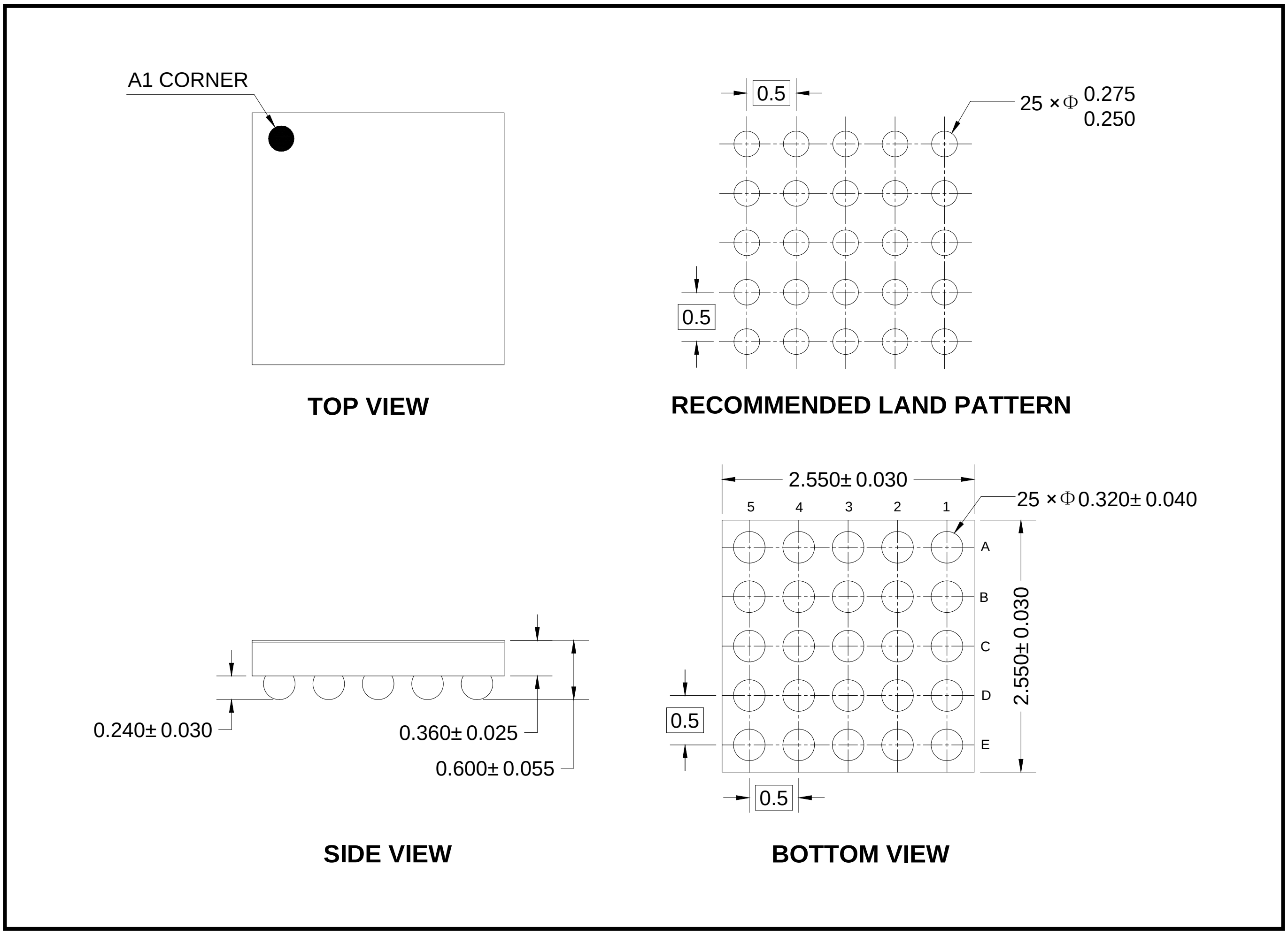
NOVEMBER 2021 – REV.A.1 to REV.A.2	Page
Updated Electrical Characteristics and Over-Voltage Protection sections	4, 14

DECEMBER 2020 – REV.A to REV.A.1	Page
Updated Programming the Limits section	17

Changes from Original (SEPTEMBER 2020) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

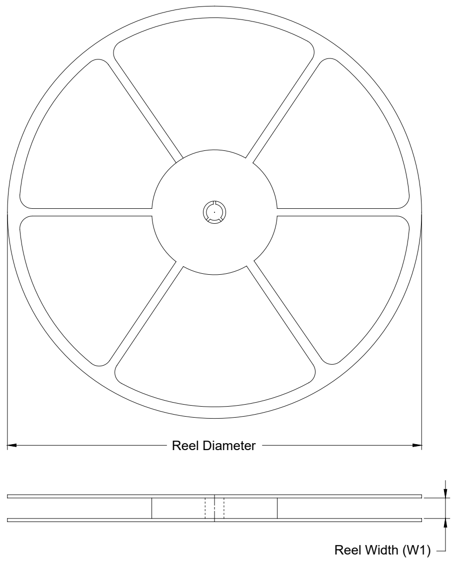
WLCSP-2.55×2.55-25B



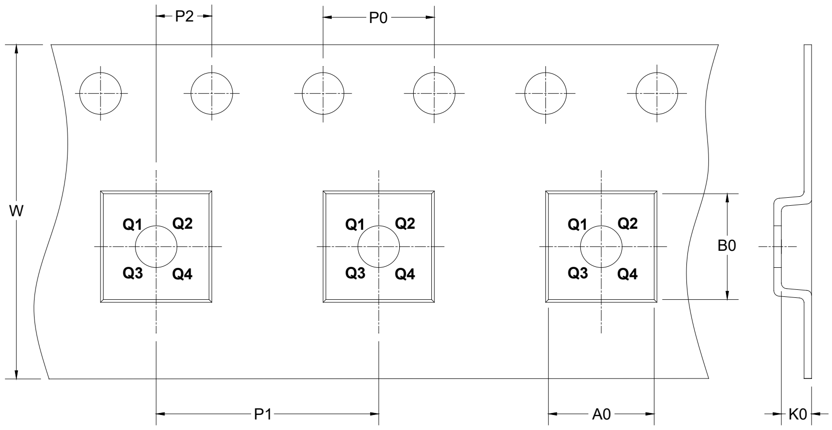
NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

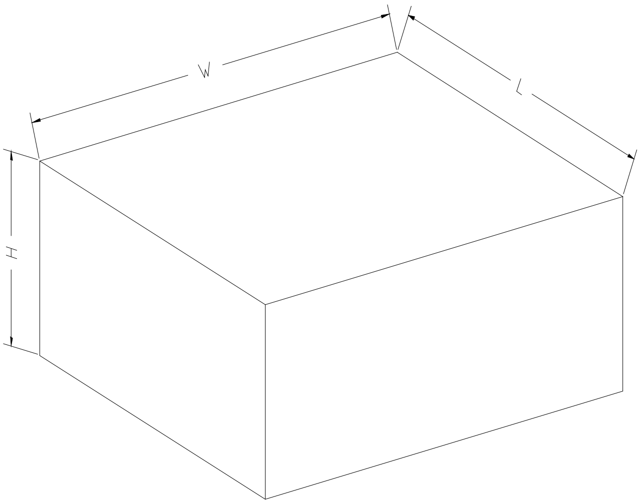
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.55×2.55-25B	13″	12.4	2.66	2.69	0.77	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002