SGM25706
60V, 6A Power Limiting, Surge Protection Industrial eFuse

GENERAL DESCRIPTION

The SGM25706 is a feature-rich 60V, 6A eFuse integrated with a 28mΩ on-resistance MOSFET. The device provides a BGATE pin to drive an external N-MOSFET which can be connected with the internal MOSFET for reverse current blocking (RCB) and input reverse polarity protection (RPP). Besides, the SGM25706 provides other functions such as under-voltage lockout (UVLO), over-voltage protection (OVP), adjustable over-current protection (OCP), fast short-circuit protection (SCP) and adjustable output slew rate control.

The SGM25706 provides fault indicator (nFLT) pin and accurate load current monitor for system monitoring and downstream load management. Besides, the power good (PG) pin can be used to control the downstream converters. The MODE pin allows the user to configure the device response under current limit faults (latch-off or auto-retry).

The SGM25706 is available in a Green TQFN-4×4-24L package.

APPLICATIONS

Industrial Automation and Control
Motor Drivers
System Circuit Breakers

TYPICAL APPLICATION

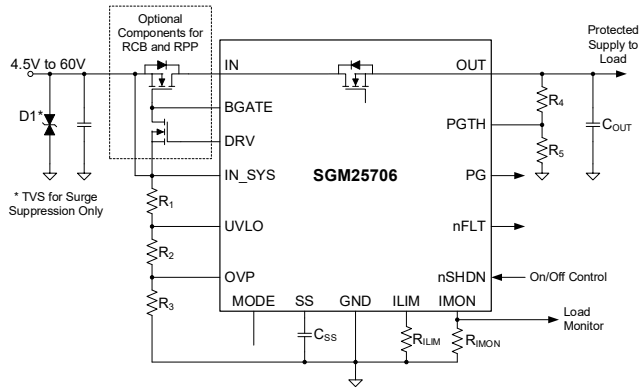


Figure 1. Typical Application Circuit

FEATURES

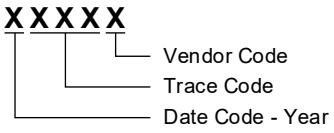
- **4.5V to 60V Operating Voltage, 67V Absolute Maximum**
- **Integrated 60V, 28mΩ On-Resistance MOSFET**
- **Support Reverse Polarity Protection (RPP) and Reverse Current Blocking (RCB) with an External N-MOSFET**
- **0.6A to 6A Adjustable Current Limit**
- **Fast Reverse Current Blocking: 0.183μs**
- **Adjustable Output Power Limiting Variants**
- **Adjustable UVLO, OVLO, Output Slew Rate Control for Inrush Current Control**
- **Able to Drive Large and Unknown Capacitive Loads by Employing Thermal Regulation during Device Power-Up**
- **Variants with 34.7V and 38.4V Maximum Over-Voltage Clamp**
- **Power Good Indicator (PG)**
- **Selectable Options for Over-Current Fault Response Offering a Choice between Auto-Retry and Latch-Off**
- **Variants with 2 × Pulse Over-Current Support**
- **Analog Current Monitor (IMON) Output**
- **Available in a Green TQFN-4×4-24L Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25706A	TQFN-4×4-24L	-40℃ to +125℃	SGM25706AXTQF24G/TR	SGM169 XTQF24 XXXXX	Tape and Reel, 3000
SGM25706B	TQFN-4×4-24L	-40℃ to +125℃	SGM25706BXTQF24G/TR	SGM16A XTQF24 XXXXX	Tape and Reel, 3000
SGM25706C	TQFN-4×4-24L	-40℃ to +125℃	SGM25706CXTQF24G/TR	SGM16B XTQF24 XXXXX	Tape and Reel, 3000
SGM25706D	TQFN-4×4-24L	-40℃ to +125℃	SGM25706DXTQF24G/TR	SGM16C XTQF24 XXXXX	Tape and Reel, 3000
SGM25706E	TQFN-4×4-24L	-40℃ to +125℃	SGM25706EXTQF24G/TR	SGM0NI XTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE COMPARISON TABLE

Model	Over-Voltage Protection	Overload Fault Response	Adjustable Output Power Limiting
SGM25706A	Over-Voltage Cut-Off, Adjustable	Active Current Limit (1 ×)	No
SGM25706B		Active Current Limit with Pulse Current Support (2 ×)	No
SGM25706C	Over-Voltage Clamp, Fixed 34.7V (MAX)	Active Current Limit (1 ×)	Yes
SGM25706D		Active Current Limit with Pulse Current Support (2 ×)	Yes
SGM25706E	Over-Voltage Clamp, Fixed 38.4V (MAX)	Active Current Limit with Pulse Current Support (2 ×)	Yes

DEVICE OPERATIONAL VARIATIONS WITH DIFFERENT MODE CONFIGURATIONS

Model	MODE Pin Configuration	Overload Protection Operation
SGM25706A, SGM25706C	Open	Active current limit at 1 × I_{OL} for a maximum duration of $t_{CL\_PLIM\_DLY}$, then latches off. Reset the device by setting the nSHDN from low to high, UVLO from low to high, or power cycling IN_SYS.
SGM25706B, SGM25706D, SGM25706E		Active current limit at 2 × I_{OL} for t_{CB_DLY} followed with current limit at 1 × I_{OL} for a maximum duration of $t_{CL\_PLIM\_DLY}$, then latches off. Reset the device by setting the nSHDN from low to high, UVLO from low to high, or power cycling IN_SYS.
SGM25706A, SGM25706C	Shorted to GND	Active current limit at 1 × I_{OL} for a maximum duration of $t_{CL\_PLIM\_DLY}$, then auto retries after a delay of t_{TSD_RETRY}.
SGM25706B, SGM25706D, SGM25706E		Active current limit at 2 × I_{OL} for t_{CB_DLY} followed with current limit at 1 × I_{OL} for a maximum duration of $t_{CL\_PLIM\_DLY}$, then auto retries after a delay of t_{TSD_RETRY}.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
IN_SYS ..... -60V to 67V
IN_SYS (10ms Transient), T_A = +25℃ ..... -60V to 75V
IN, OUT, UVLO, nFLT, PG, PGTH ..... -0.3V to 67V
IN_SYS - OUT (10ms Transient), with a Blocking MOSFET..
..... ≥ -85V
IN (10ms Transient), T_A = +25℃..... -0.3V to 75V
BGATE..... -60V to 81V
BGATE - IN_SYS..... -0.3V to 15V
DRV ..... -60V to 72V
DRV - IN_SYS ..... -0.3V to 7.5V
OVP, SS, IMON, MODE, nSHDN, ILIM, PLIM.....
..... -0.3V to 5.5V
Sink Current
I_{nFLT}, I_{SS}, I_{PG} 10mA
Source Current
I_{SS}, I_{ILIM}, I_{PLIM}, I_{MODE}, I_{nSHDN} ..... Internally Limited
Package Thermal Resistance
TQFN-4×4-24L, θ_{JA}..... 36.7℃/W
TQFN-4×4-24L, θ_{JB}..... 15.5℃/W
TQFN-4×4-24L, $\theta_{JC\ (TOP)}$..... 26.2℃/W
TQFN-4×4-24L, $\theta_{JC\ (BOT)}$..... 12.4℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage
IN_SYS, IN .....4.5V to 60V
OUT, UVLO, PGTH, PG, nFLT..... 0V to 60V
OVP, SS, IMON, MODE..... 0V to 4V
nSHDN ..... 0V to 5V
Resistance
ILIM .....3kΩ to 30kΩ
IMON..... ≥ 1kΩ
PLIM.....60.4kΩ to 150kΩ
External Capacitance
IN, IN_SYS, OUT .....≥ 0.1μF
SS .....≥ 10nF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

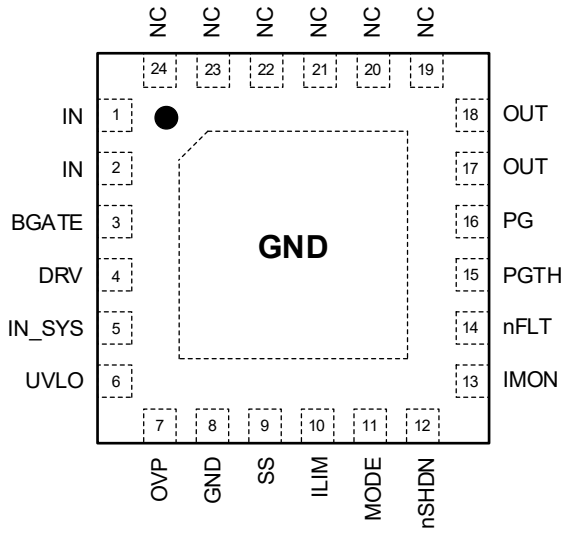
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

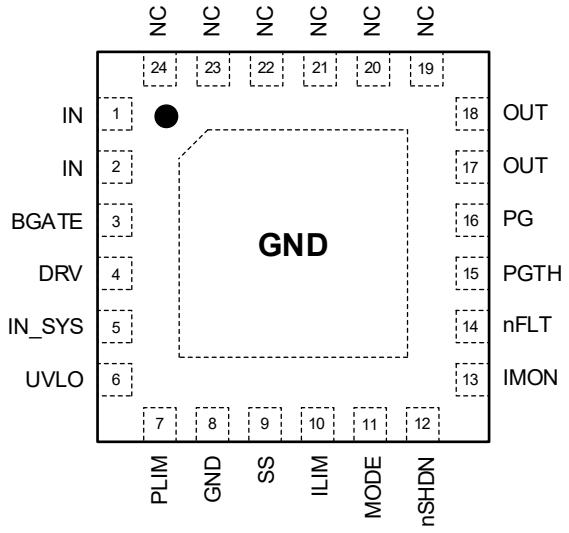
PIN CONFIGURATIONS

SGM25706A/B (TOP VIEW)



TQFN-4×4-24L

SGM25706C/D/E (TOP VIEW)



TQFN-4×4-24L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 2	IN	P	Device Power Input.
3	BGATE	O	Gate Driver Output for External Blocking MOSFET. Connect this pin to the external MOSFET GATE. If the external MOSFET is not used, float this pin.
4	DRV	O	Gate Driver Output for Fast Pull-Down Switch MOSFET. Connect this pin to the external pull-down switch GATE. If the external MOSFET is not used, float this pin.
5	IN_SYS	P	Power Input and Supply Voltage of the Device. Connect this pin to the external MOSFET source if the MOSFET is used. If the external MOSFET is not used, short IN_SYS pin to IN pin.
6	UVLO	I	Under-Voltage Lockout Setting Pin. An under-voltage event on this pin turns off the internal MOSFET and asserts the nFLT pin. Tie this pin to GND for selecting the internal default threshold.
7	OVP	I	Over-Voltage Protection Threshold Setting Pin. (For SGM25706A/B Only). An over-voltage event on this pin turns off the internal MOSFET and asserts the nFLT pin. Tie the UVLO pin to GND for selecting the internal default threshold.
	PLIM	I	Output Power Limit Threshold Setting Pin. (For SGM25706C/D/E Only). Connect this pin to GND through a resistor to set the output power limit. If the output power limit feature is not used, connect this pin to GND.
8	GND	—	Device Ground. Connect this pin to System Ground.
9	SS	I/O	Soft-Start Pin. Place a capacitor from this pin to GND to set the output voltage slew rate.
10	ILIM	I/O	Current Limit Programming Pin. Place a resistor from this pin to GND to set the over-current and short-circuit current limit.
11	MODE	I	Over-Current Fault Response Mode Selection Pin.
12	nSHDN	I	Device Shutdown Pin (Active Low). Pulling this pin low activates the low power shutdown mode. Cycle this pin to reset the device that has latched off due to a fault condition.
13	IMON	O	Current Monitor Pin. The sourcing current of this pin is proportional to the MOSFET current. Placing a resistor from this pin to GND transforms the current to voltage signal. If not used, float this pin.
14	nFLT	O	Fault Event Indicator with an Open-Drain Structure. If this pin is not used, float the pin or tie it to GND.
15	PGTH	I	Power Good Comparator Input.
16	PG	O	Power Good Indicator (Active High). This pin is asserted high when the voltage at PGTH has reached the V_{PGTHR} threshold and the internal MOSFET is fully turned on. This pin goes low when V_{PGTH} drops below V_{PGTHF} threshold. If this pin is not used, float the pin or tie it to GND.
17, 18	OUT	P	Device Power Output.
19, 20, 21, 22, 23, 24	NC	—	No Connection.
Exposed Pad	GND	—	The GND terminal must be connected to the exposed pad, which needs to be connected through numerous vias to a PCB ground plane for effective thermal performance.

NOTE: P = power, I = input, O = output, I/O = input/output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 4.5V to 60V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = open, C_{SS} = open. All voltages are with respect to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Operating Input Voltage	V_{IN_SYS}		4.5		60	V
Supply Current	I_{Q_ON}	Enabled: V_{nSHDN} = 2V, V_{UVLO} = 2V		280	430	μA
	I_{Q_OFF}	V_{nSHDN} = 2V, V_{UVLO} = 1V		58	130	
		V_{nSHDN} = 0V, V_{UVLO} = 0V		19	50	
Ground Current during Reverse Polarity	I_{GND}	V_{IN_SYS} = -24V, V_{IN} = floating, V_{OUT} = 0V		0.6	1.6	mA
Over-Voltage Clamp	V_{OVC}	V_{IN_SYS} > 35V, SGM25706C/D only	31.7	33.2	34.7	V
		V_{IN_SYS} > 40V, SGM25706E only	35.6	37	38.4	V
Under-Voltage Lockout (UVLO) Input						
Factory Set V_{IN_SYS} Under-Voltage Trip Level	V_{INSYS_UVLO}	V_{IN_SYS} rising, V_{UVLO} = 0V	15	15.38	15.8	V
		V_{IN_SYS} falling, V_{UVLO} = 0V	14	14.45	14.9	V
Internal UVLO Select Threshold	V_{SEL_UVLO}		190	212	230	mV
UVLO Threshold Voltage, Rising	V_{UVLOR}		1.163	1.2	1.229	V
UVLO Threshold Voltage, Falling	V_{UVLOF}		1.094	1.122	1.146	V
UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to 60V	-150	10	150	nA
Over-Voltage Protection (OVP) Input						
Factory Set V_{IN_SYS} Over-Voltage Trip Level	$V_{IN\_SYS\_OVP}$	V_{IN_SYS} rising, V_{OVP} = 0V	33.1	34.16	35.2	V
		V_{IN_SYS} falling, V_{OVP} = 0V	32.6	33.67	34.7	V
Internal OVP Select Threshold	V_{SEL_OVP}		190	212	230	mV
Over-Voltage Threshold Voltage, Rising	V_{OVPR}		1.163	1.2	1.229	V
Over-Voltage Threshold Voltage, Falling	V_{OVPF}		1.094	1.122	1.146	V
OVP Input Leakage Current	I_{OVP}	V_{OVP} = 0V to 4V	-150	0	150	nA
Current Limit Programming (ILIM)						
Overload Current Limit	I_{OL}	R_{ILIM} = 30kΩ, V_{IN} - V_{OUT} = 1V, V_{IN_SYS} = 24V	0.47	0.59	0.71	A
		R_{ILIM} = 9kΩ, V_{IN} - V_{OUT} = 1V, V_{IN_SYS} = 24V	1.78	2	2.18	A
		R_{ILIM} = 4.02kΩ, V_{IN} - V_{OUT} = 1V, V_{IN_SYS} = 24V	4.22	4.5	4.77	A
		R_{ILIM} = 3kΩ, V_{IN} - V_{OUT} = 1V, V_{IN_SYS} = 24V	5.59	6	6.55	A
Transient Pulse Over-Current Limit	I_{OL_Pulse}	R_{ILIM} = 3kΩ to 30kΩ, SGM25706B/D/E only		2 × I_{OL}		A
Fast-Trip Comparator Threshold	$I_{FASTTRIP}$	SGM25706A/C		2 × I_{OL}		A
		SGM25706B/D/E only		3 × I_{OL}		A
Short-Circuit Protect Current	I_{SCP}			37		A
Output Power Limiting Control (PLIM) Input: SGM25706C/D/E Only						
Power Limit Feature Select Threshold	V_{SEL_PLIM}		190	212	230	mV
PLIM Sourcing Current	I_{PLIM}	V_{PLIM} = 0V	3.9	4.97	6	μA
Max Output Power	P_{PLIM}	R_{PLIM} = 60.4kΩ, T_J = +25℃	59	63	67.5	W
		R_{PLIM} = 60.4kΩ, T_J = -40℃ to +125℃	49	63	77.3	
		R_{PLIM} = 100kΩ, T_J = +25℃	104	110	115	
		R_{PLIM} = 100kΩ, T_J = -40℃ to +125℃	88	110	132	
		R_{PLIM} = 150kΩ, T_J = +25℃	154	180	212	
		R_{PLIM} = 150kΩ, T_J = -40℃ to +125℃	130	180	235	
BGATE (Blocking MOSFET Gate Driver)						
BGATE Clamp Voltage	V_{BGATE}	V_{BGATE} - V_{IN_SYS}, V_{IN_SYS} = 24V	9	10.08	11	V
Blocking MOSFET Gate Drive Current	I_{BGATE}	V_{BGATE} - V_{IN_SYS} = 1V	16.3	19.61	22.7	μA
BGATE Pull-Down Resistance (1)	R_{PD_BGATE}		500	843	1150	kΩ
DRV Logic High Level	V_{DRV_OH}	V_{DRV} - V_{IN_SYS}, V_{IN_SYS} = 24V	3	4.71	5.2	V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 4.5V to 60V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = open, C_{SS} = open. All voltages are with respect to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pass MOSFET Output (OUT)						
IN to OUT Total On-Resistance	R_{DSON}	I_{OUT} = 2A, T_J = +25℃	23	27.64	33.5	mΩ
		I_{OUT} = 2A, T_J = -40℃ to +85℃		27.64	44	
		I_{OUT} = 2A, T_J = -40℃ to +125℃		27.64	52	
OUT Leakage during Input Supply Brownout	I_{LKGOUT}	V_{IN_SYS} = 0V, V_{OUT} = 24V, V_{IN} = floating, V_{nSHDN} = 2V, sinking	-30			μA
V_{IN_SYS} - V_{OUT} Rising Threshold for Reverse Protection Comparator	V_{REVTH}		-20	-14	-9	mV
V_{IN_SYS} - V_{OUT} Falling Threshold for Reverse Protection Comparator	V_{FWDTH}	V_{IN_SYS} ≥ 5.0V	42	58	75	mV
Output Ramp Control (SS)						
SS Charging Current	I_{SS}	V_{SS} = 0V	1.43	1.96	2.47	μA
SS to OUT Gain	$GAIN_{SS}$	V_{OUT}/V_{SS}, V_{IN_SYS} = 24V	24.4	25	25.5	V/V
SS Maximum Capacitor Voltage	V_{SS_MAX}		4	4.3	4.6	V
SS Discharging Resistance	R_{SS}		11	20.3	29	Ω
Low I_Q Shutdown (nSHDN) Input						
Open Circuit Voltage	V_{nSHDN}	I_{nSHDN} = 0.1μA	4.1	4.3	4.5	V
nSHDN Threshold Voltage for Low I_Q Shutdown, Falling	V_{nSHUTF}		0.8			V
nSHDN Threshold Rising	V_{nSHUTR}				1.8	V
Leakage Current	I_{nSHDN}	V_{nSHDN} = 0V	-8			μA
Current Monitor Output (IMON)						
Gain Factor I_{IMON}:I_{OUT}	$GAIN_{IMON}$	I_{OUT} = 0.6A, V_{IN_SYS} = 24V	25.17	27.51	29.86	μA/A
		I_{OUT} = 1A, V_{IN_SYS} = 24V	25.7	27.7	29.7	
		I_{OUT} = 2A, V_{IN_SYS} = 24V	26.23	27.83	29.44	
		I_{OUT} = 3A, V_{IN_SYS} = 24V	26.48	27.88	29.27	
		I_{OUT} = 4A, V_{IN_SYS} = 24V	26.61	27.9	29.2	
		I_{OUT} = 5A, V_{IN_SYS} = 24V	26.69	27.92	29.17	
		I_{OUT} = 6A, V_{IN_SYS} = 24V	26.7	27.94	29.22	
FAULT FLAG (nFLT): Active-Low						
nFLT Pull-Down Resistance	R_{nFLT}		50	79	110	Ω
nFLT Input Leakage Current	I_{nFLT}	V_{nFLT} = 0V to 60V	-150	6	150	nA
Power Good (PG)						
PG Pull-Down Resistance	R_{PG}		50	78	110	Ω
PG Input Leakage Current	I_{PG}	V_{PG} = 0V to 60V	-150	6	150	nA
Positive Input for Power Good Comparator (PGTH)						
PGTH Threshold Voltage, Rising	V_{PGTHR}		1.163	1.2	1.229	V
PGTH Threshold Voltage, Falling	V_{PGTHF}		1.094	1.122	1.146	V
PGTH Input Leakage Current	I_{PG}	V_{PGTH} = 0V to 60V	-150	6	150	nA
Thermal Protection						
Thermal Regulation Set Point	T_{J_REG}			130		℃
Thermal Shutdown Threshold, Rising	T_{SD}			167		℃
Thermal Shutdown Hysteresis	T_{HYS}			16		℃
MODE						
Mode Selection		MODE = open	Latch-Off			
		MODE = short to GND	Auto-Retry			

NOTE:

1. Guaranteed by design, not verified in production testing.

TIMING REQUIREMENTS

(T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 4.5V to 60V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = open, C_{SS} = open. All voltages are with respect to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Input (UVLO)						
UVLO Switch Turn-On Delay	$t_{UVLO\_ON\_DLY}$	UVLO↑ (200mV above V_{UVLOR}) to V_{OUT} = 200mV with V_{PGTH} = low, C_{SS} = 10nF		1270		μs
UVLO Switch Turn-On Delay (Fast)	$t_{UVLO\_ON\_FAST\_DLY}$	UVLO↑ (200mV above V_{UVLOR}) to V_{OUT} = 200mV with V_{PGTH} = high	65	115	210	μs
UVLO Switch Turn-Off Delay	$t_{UVLO\_OFF\_DLY}$	UVLO↓ (100mV below V_{UVLOF}) to nFLT↓ 10%	2	4	7.8	μs
UVLO to Fault De-assertion Delay	$t_{UVLO\_nFLT\_DLY}$	UVLO↑ to nFLT↑ delay	560	753	960	μs
Over-Voltage Protection Input (OVP)						
OVP Switch Turn-Off Delay	$t_{OVP\_OFF\_DLY}$	OVP↑ (200mV above V_{OVPR}) to nFLT↓	1	2	3.4	μs
OVP Switch Turn-On Delay (Fast)	$t_{OVP\_ON\_FAST\_DLY}$	OVP↓ (100mV below V_{OVPF}) to V_{OUT} = 200mV with V_{PGTH} = high	8.8	25	52.5	μs
OVP Switch Disable Delay	$t_{OVP\_ON\_DLY}$	OVP↓ (100mV below V_{OVPF}) to V_{OUT} = 200mV with V_{PGTH} = low, C_{SS} = 10nF		368		μs
Maximum Duration in Output Voltage Clamp Operation	t_{OVC_DLY}	SGM25706C/D/E only		170		ms
nFLT Assertion Delay in Output Voltage Clamp Operation	$t_{OVC\_nFLT\_DLY}$	SGM25706C/D/E only		691		μs
Shutdown Control Input (nSHDN)						
Shutdown Entry Delay	t_{SD_DLY}	nSHDN↓ (below V_{SHUTF}) to MOSFET off	1.8	4.1	5.8	μs
Current Limit						
Hot-Short Response Time	$t_{FASTTRIP\_DLY}$	I_{OUT} > I_{SCP}		0.3		μs
Soft Short Response		$I_{FASTTRIP}$ < I_{OUT} < I_{SCP}		2		μs
nFLT Delay in Current & (Power Limiting: SGM25706C Only)	t_{CB_DLY}	Current limiting: SGM25706A/C only		0.63	2.6	ms
Maximum Duration in 2 × Current Limiting & (Power Limiting: SGM25706D/E Only)		I_{OL} < I_{OUT} ≤ I_{2xOL} Current limiting: SGM25706B/D/E only	19.5	26.3	33.5	ms
Maximum Duration in Current & (Power Limiting: SGM25706C/D/E Only)	$t_{CL\_PLIM\_DLY}$		125	171	220	ms
Retry Delay in Pulse Over-Current Limiting & (Power Limiting: SGM25706C/D/E Only)	$t_{CBRETRY\_DLY}$	MODE = GND	500	682	860	ms
Reverse Current Blocking (RCB) Comparator						
Reverse Protection Comparator Detection Delay (Reverse)	$t_{RCB\_FAST\_DLY}$	(V_{IN_SYS} - V_{OUT})↓ (1V overdrive below V_{REVTH}) to V_{DRV}↑		0.183	0.3	μs
Fault Assertion Delay	$t_{RCB\_FLT\_DLY}$	(V_{IN_SYS} - V_{OUT})↓ to nFLT↓	470	661	839	μs
Reverse Protection Comparator Detection Delay (Forward)	$t_{FWD\_FLT\_DLY}$	(V_{IN_SYS} - V_{OUT})↑ to V_{BGATE} - V_{IN_SYS} = 5V, $C_{BFET\text{-}IN\_SYS}$ = 4.7nF		1.33		ms
Fault De-Assertion Delay		(V_{IN_SYS} - V_{OUT})↑ to nFLT↑	475	767	1190	μs
Output Ramp Control (SS)						
Output Ramp Time in Fast Charging	$t_{FASTCHARGE}$	C_{SS} = open, 10% to 90% V_{OUT}, C_{OUT} = 1μF, V_{IN} = 24V	280	418	560	μs
Output Ramp Time	t_{SS}	C_{SS} = 22nF, 10% to 90% V_{OUT}, V_{IN} = 24V		8.63		ms
Power Good (PG)						
PG Delay (Deglitch) Time	t_{PG}	Rising edge, PGTH↑ (200mV above V_{PGTHR})	0.96	1.35	1.71	ms
		Falling edge, PGTH↓ (100mV below V_{PGTHF})	0.96	1.58	2.51	μs
Fault Flag (nFLT)						
nFLT Assertion Delay in Pulse Over-Current Limiting	$t_{CB\_FLT\_DLY}$	SGM25706B/D/E only	19.5	26.3	33.5	ms
Thermal Protection						
Thermal Shutdown Auto-Retry Interval	t_{TSD_RETRY}	MODE = GND	500	682	860	ms
Thermal Regulation Timeout	$t_{TREG\_TIMEOUT}$			2.77		s

TIMING DIAGRAM

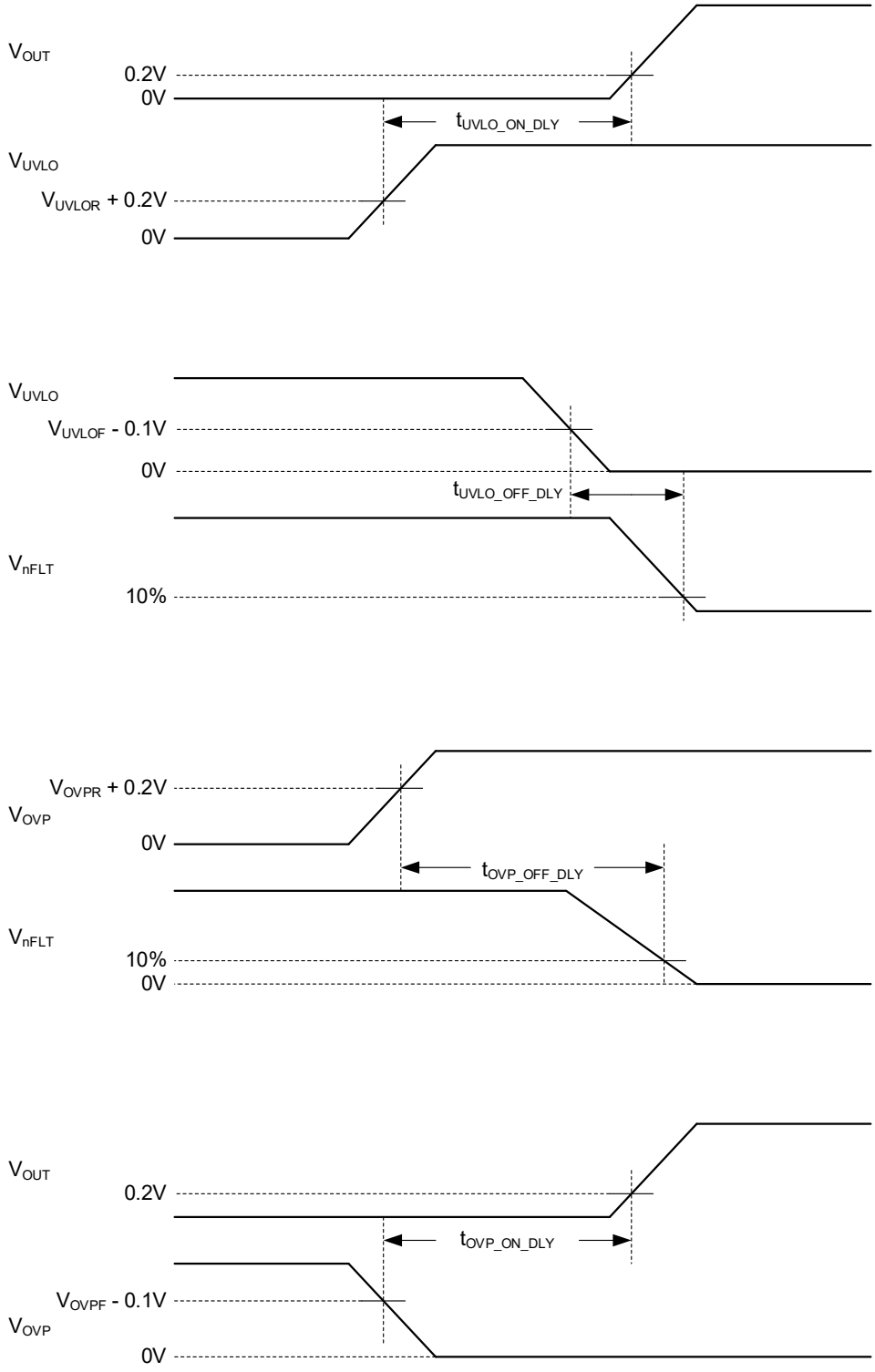


Figure 2. Timing Diagram

TIMING DIAGRAM (continued)

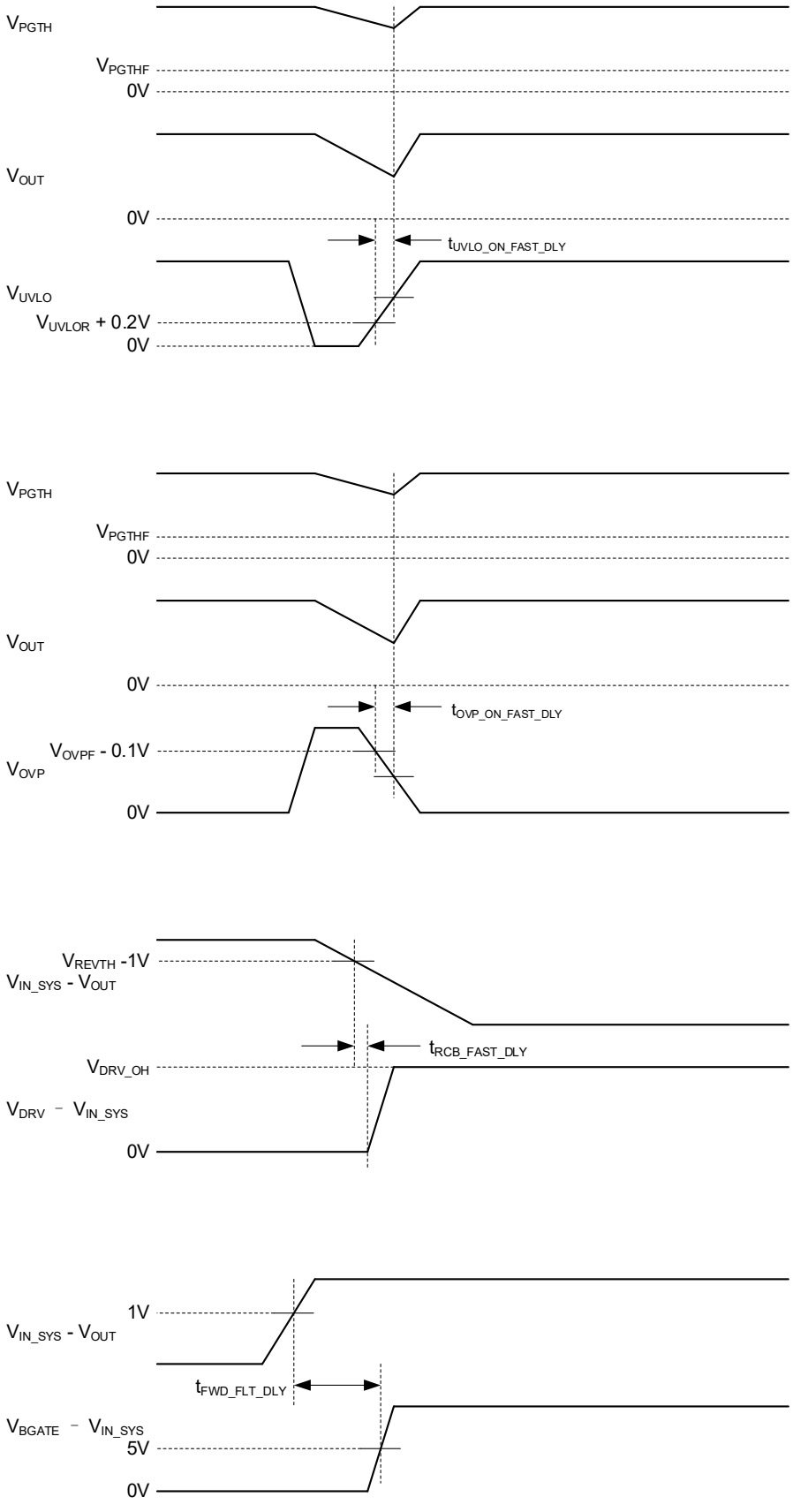


Figure 3. Timing Diagram

TIMING DIAGRAM (continued)

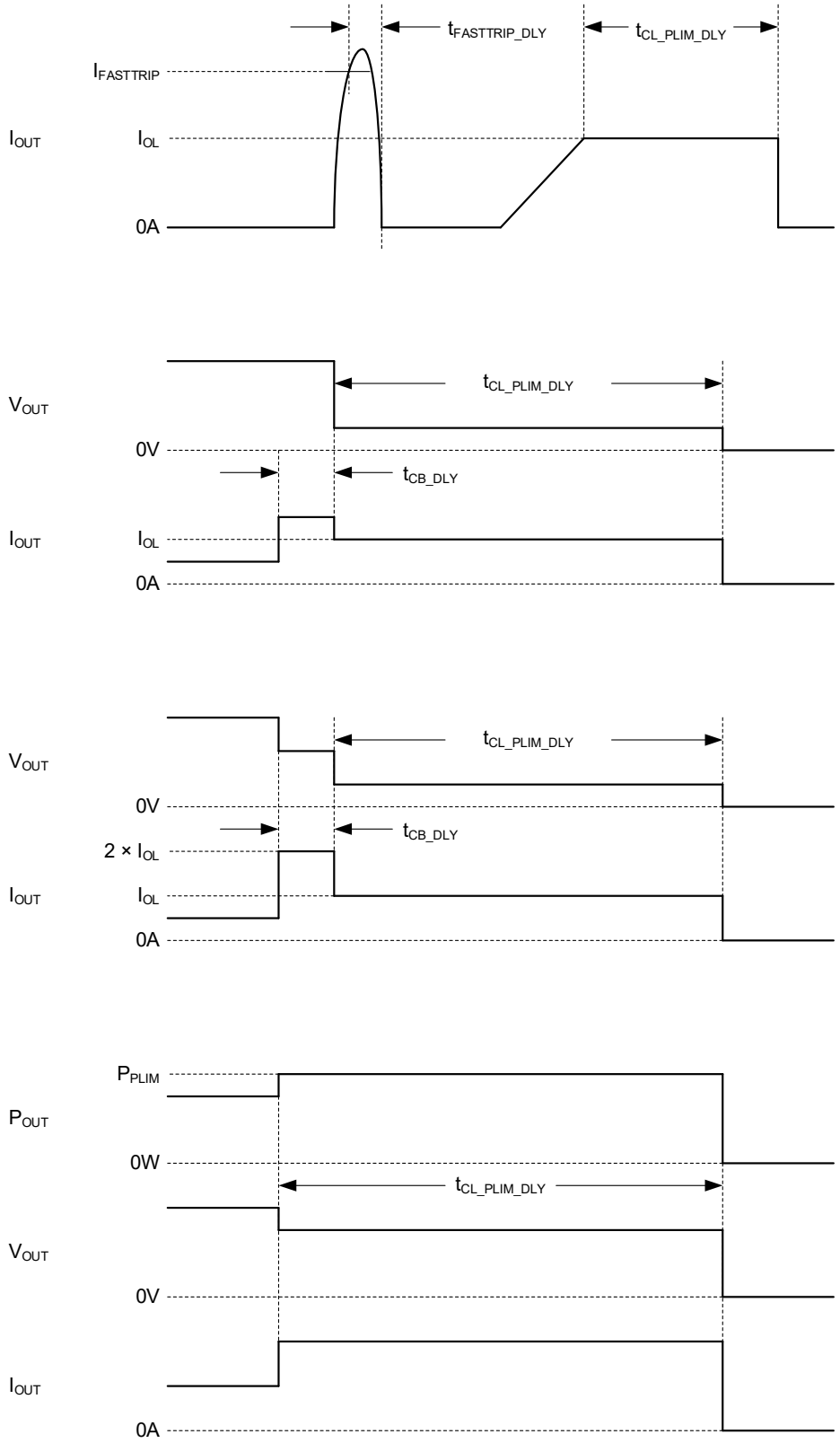
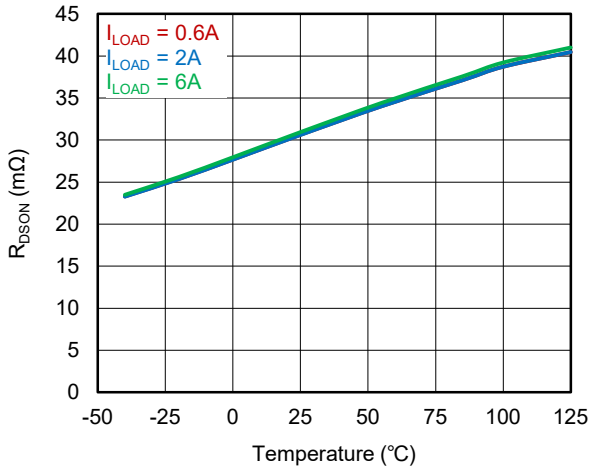


Figure 4. Timing Diagram

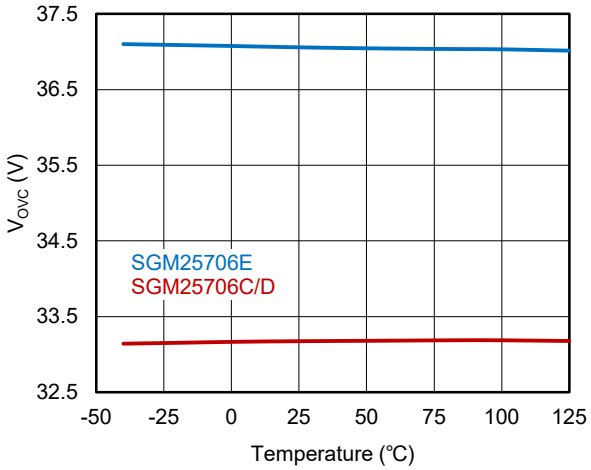
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = C_{SS} = open, unless otherwise noted.

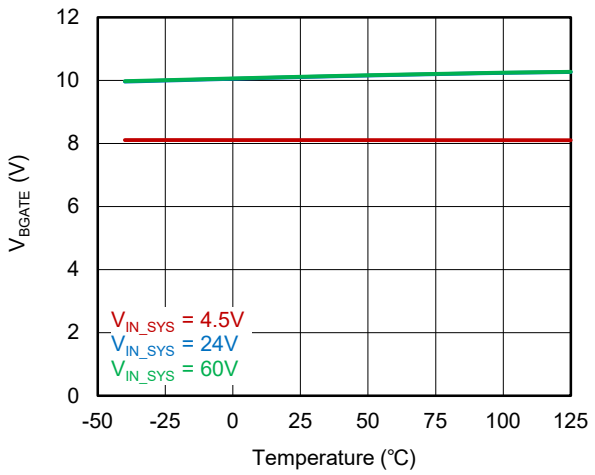
R_{DSON} vs. Temperature



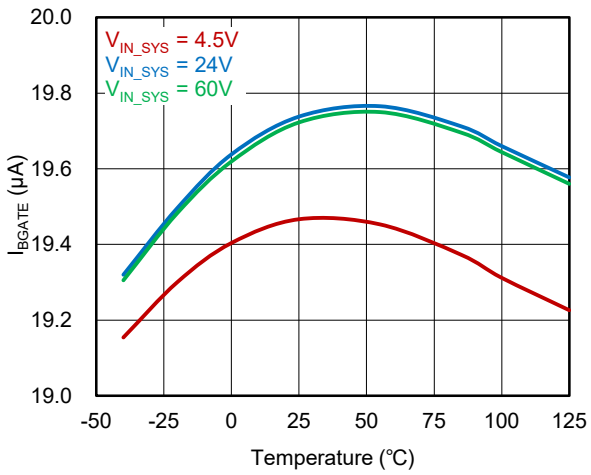
V_{OVC} vs. Temperature



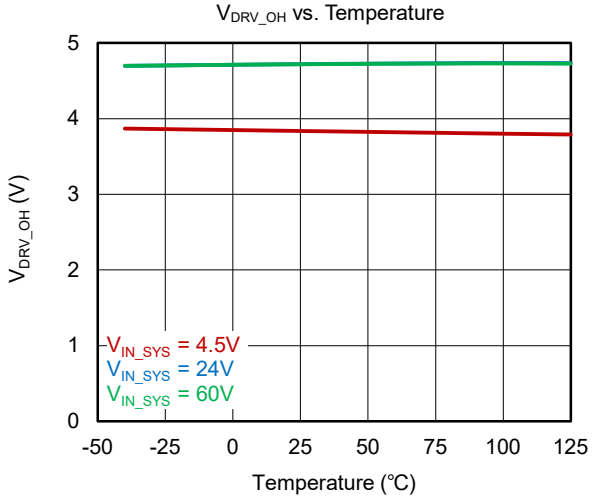
V_{BGATE} vs. Temperature



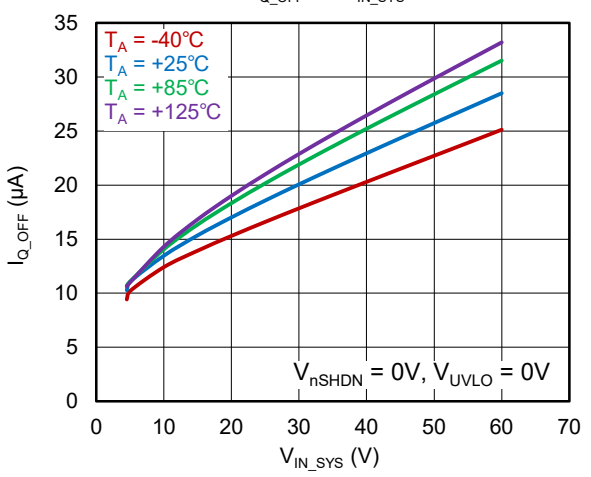
I_{BGATE} vs. Temperature



V_{DRV_OH} vs. Temperature



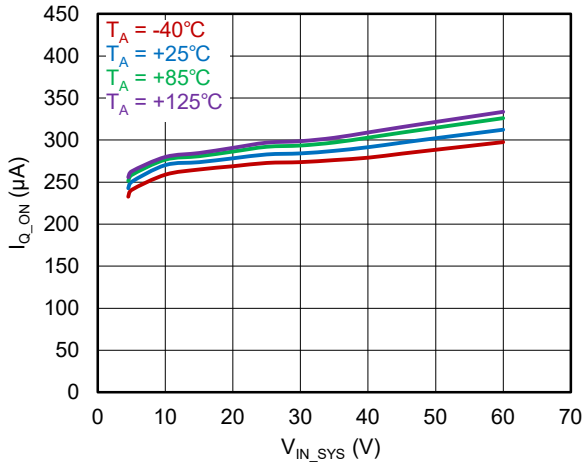
I_{Q_OFF} vs. V_{IN_SYS}



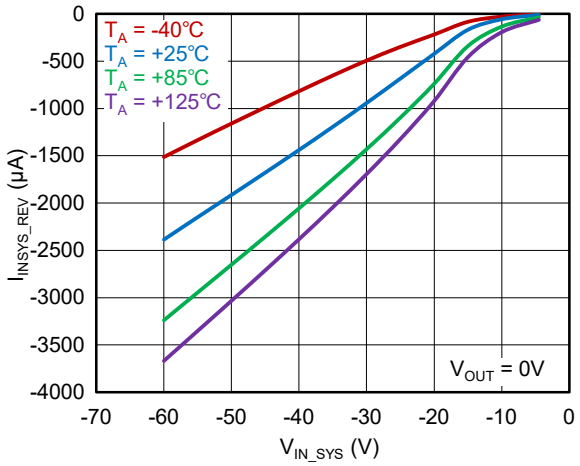
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = C_{SS} = open, unless otherwise noted.

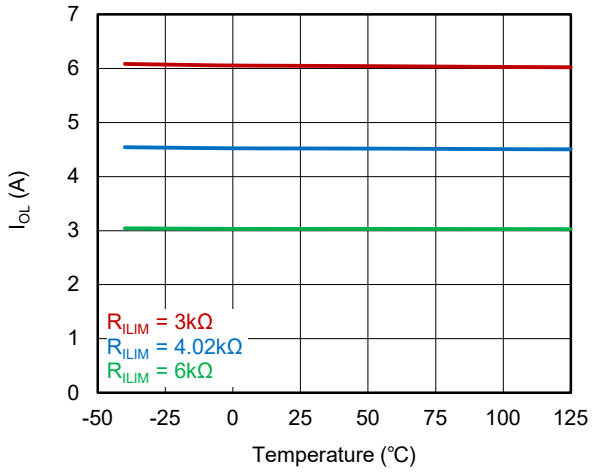
I_{Q_ON} vs. V_{IN_SYS}



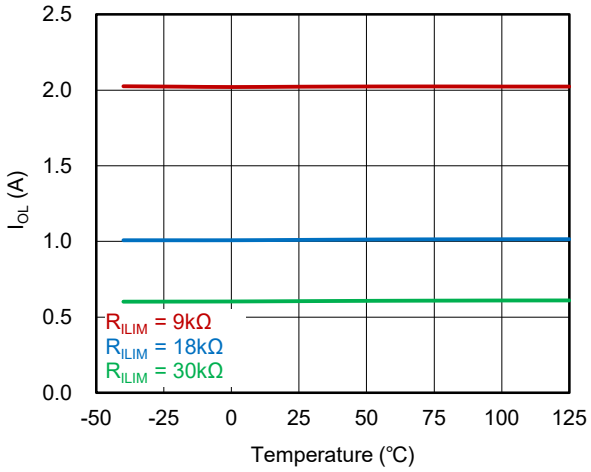
I_{INSYS_REV} vs. V_{IN_SYS}



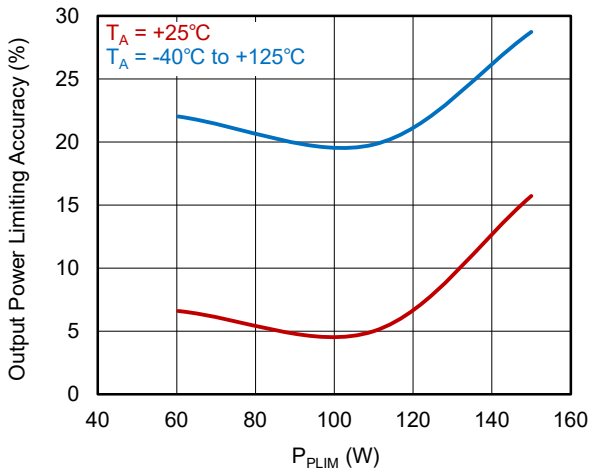
I_{OL} vs. Temperature



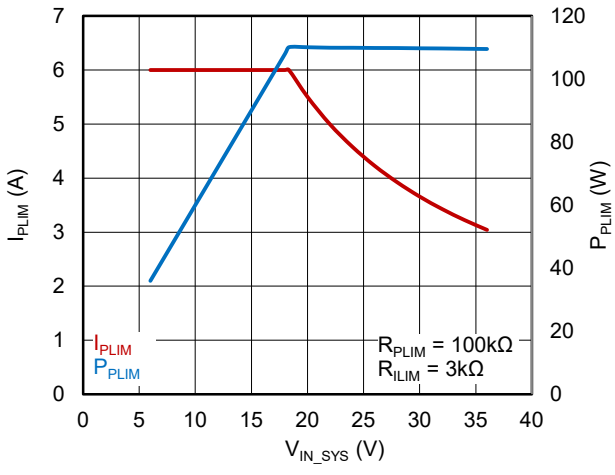
I_{OL} vs. Temperature



Output Power Limiting Accuracy vs. P_{PLIM}



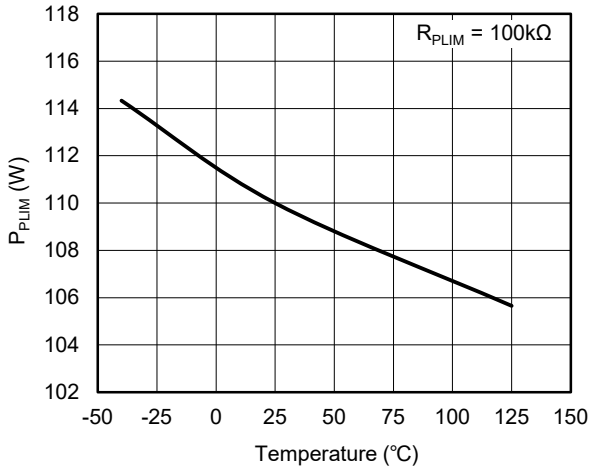
I_{PLIM}, P_{PLIM} vs. V_{IN_SYS}



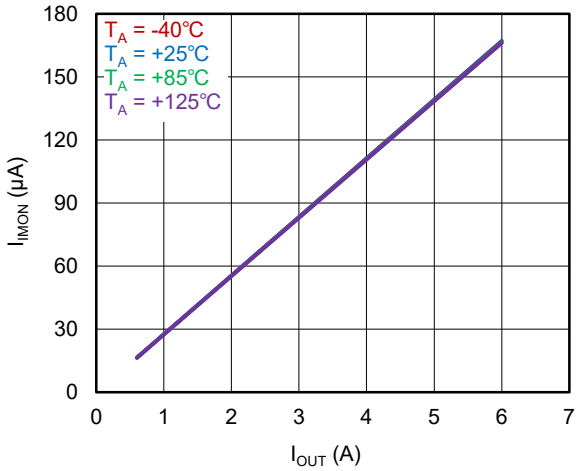
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = C_{SS} = open, unless otherwise noted.

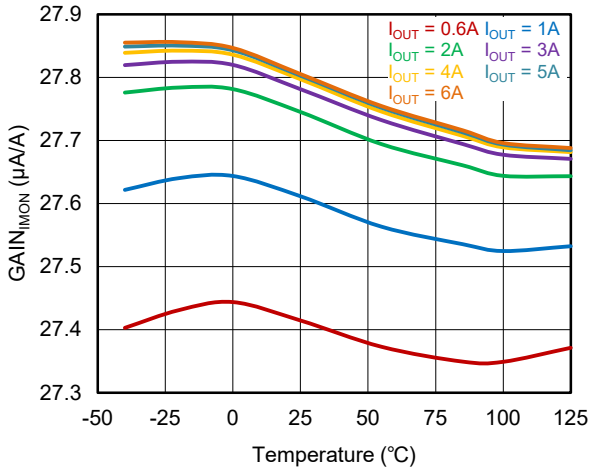
P_{PLIM} vs. Temperature



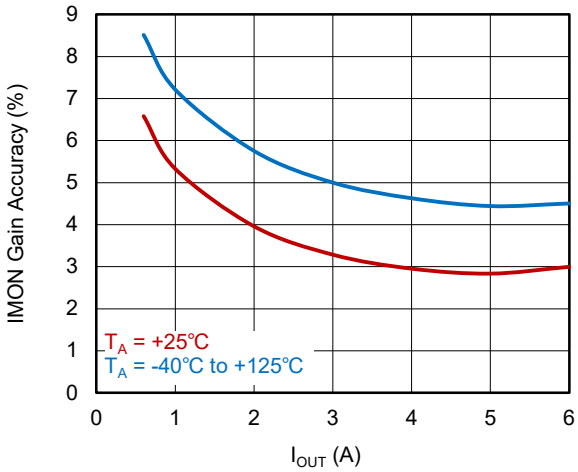
I_{IMON} vs. I_{OUT}



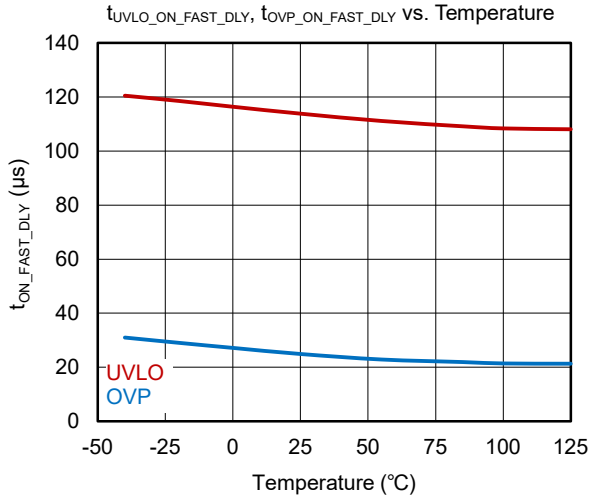
$GAIN_{IMON}$ vs. Temperature



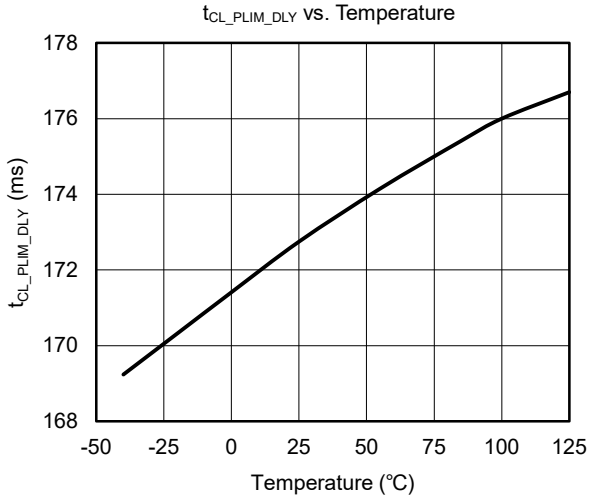
IMON Gain Accuracy vs. I_{OUT}



$t_{UVLO\_ON\_FAST\_DLY}$, $t_{OVP\_ON\_FAST\_DLY}$ vs. Temperature



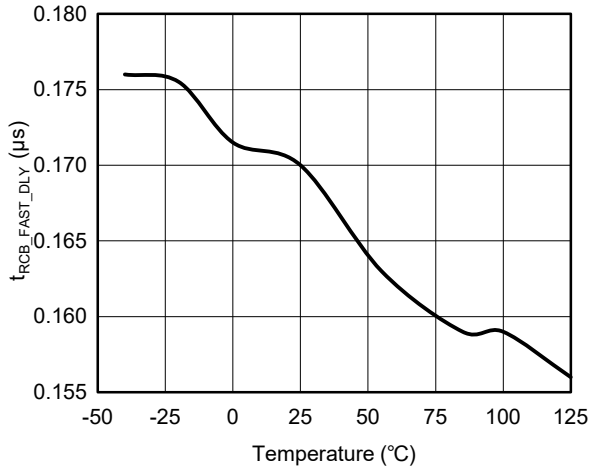
$t_{CL\_PLIM\_DLY}$ vs. Temperature



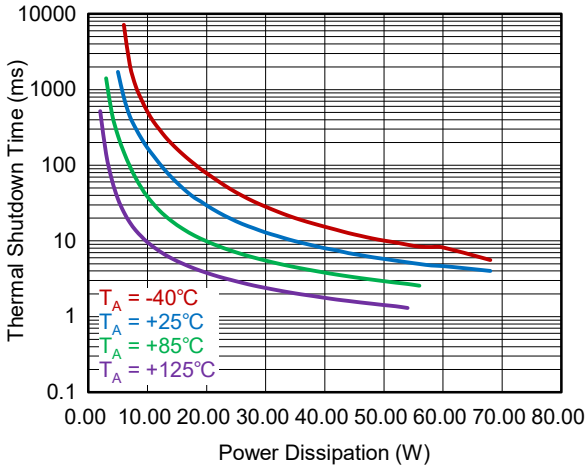
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, V_{IN_SYS} = V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 30kΩ, IMON = PG = nFLT = C_{SS} = open, unless otherwise noted.

$t_{RCB\_FAST\_DLY}$ vs. Temperature



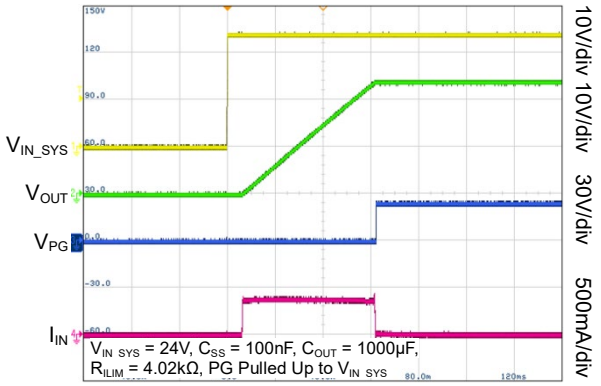
Thermal Shutdown Time vs. Power Dissipation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

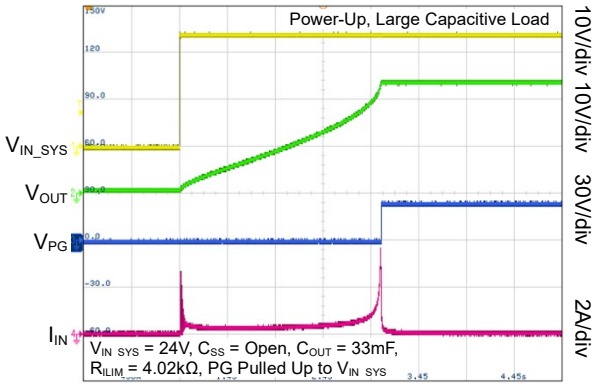
T_A = +25℃, unless otherwise noted.

Hot-Plug In and Inrush Current Control at 24V Input



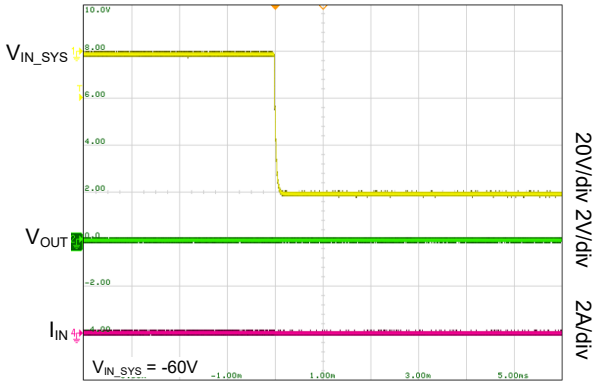
Time (20ms/div)

Thermal Regulation Loop Response



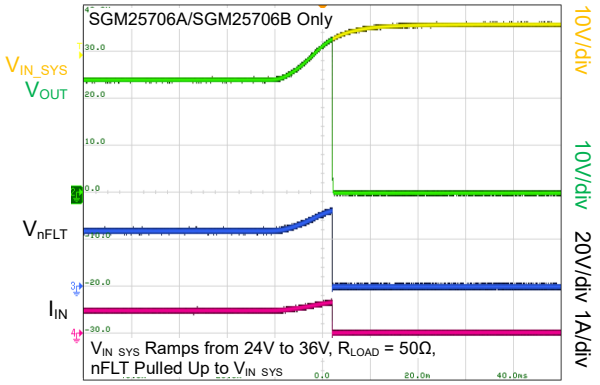
Time (500ms/div)

Input Reverse Polarity Response at -60V Input



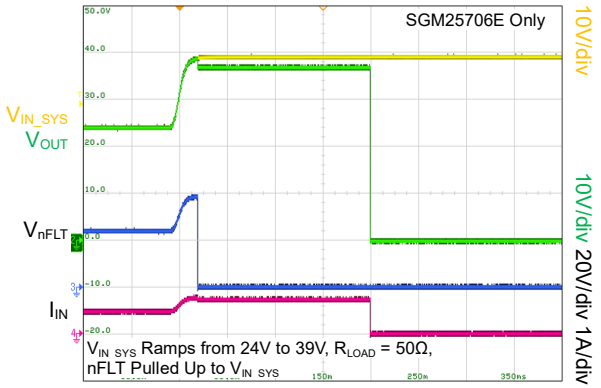
Time (1ms/div)

Over-Voltage Cut-Off Response at 33V Level



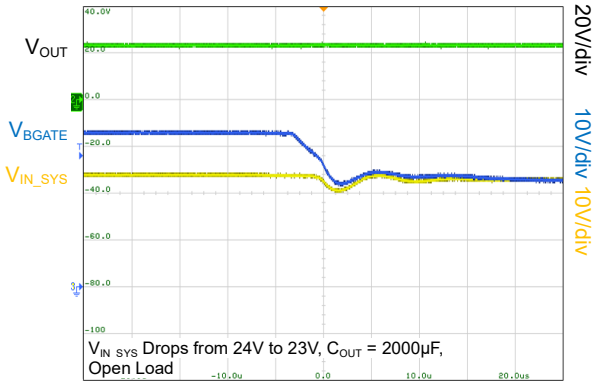
Time (10ms/div)

Over-Voltage Clamp Response



Time (50ms/div)

Reverse Current Protection Response

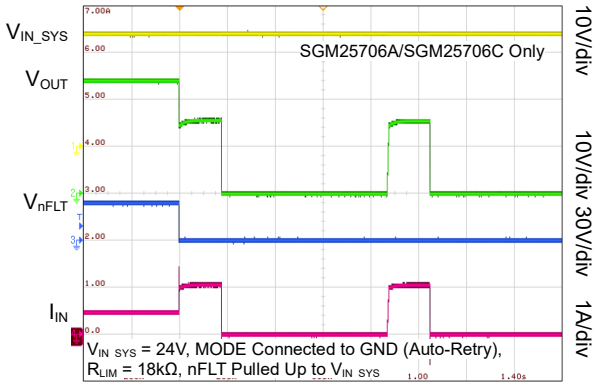


Time (5μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

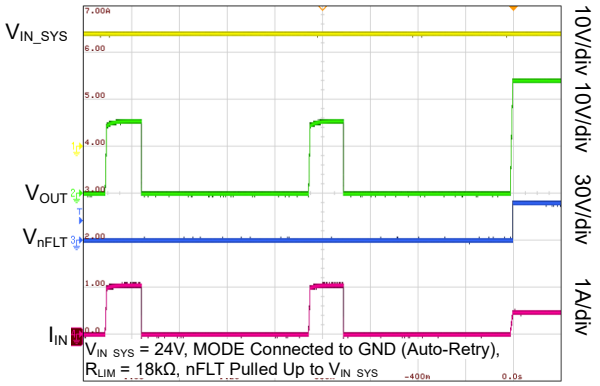
T_A = +25℃, unless otherwise noted.

Overload Performance, Load Step from 50Ω to 15Ω



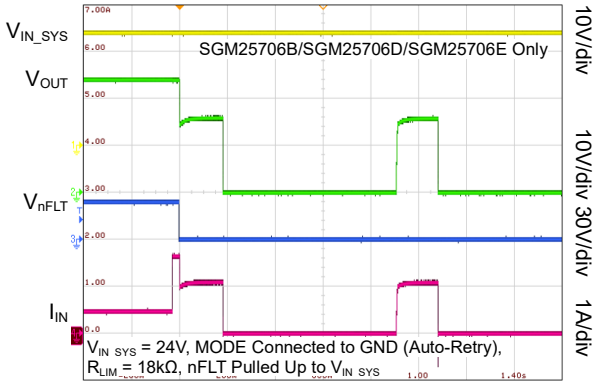
Time (200ms/div)

Recover from Overload Fault Response



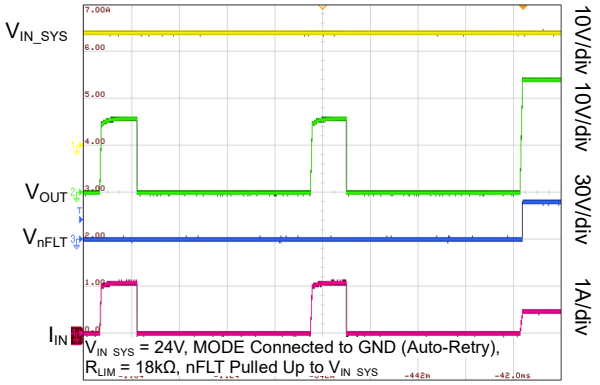
Time (200ms/div)

Overload Performance, Load Step from 50Ω to 15Ω



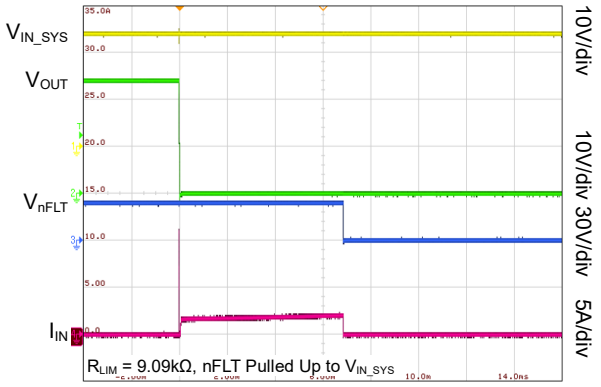
Time (200ms/div)

Response during Coming Out of Overload Fault



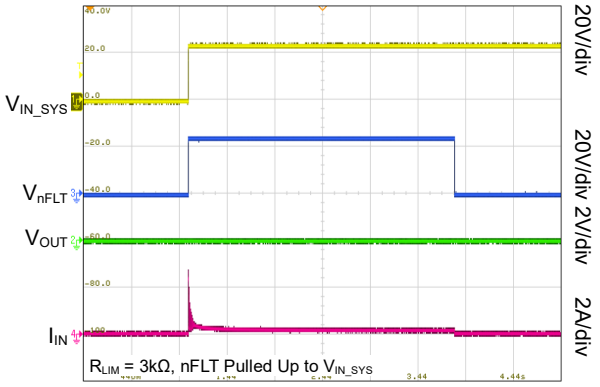
Time (200ms/div)

Output Hot-Short Response



Time (2ms/div)

Start-Up with Short on Output

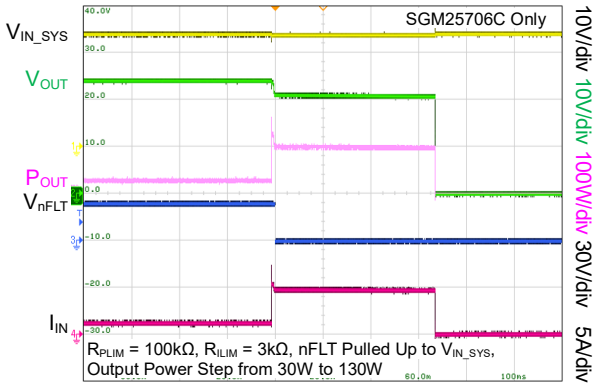


Time (500ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

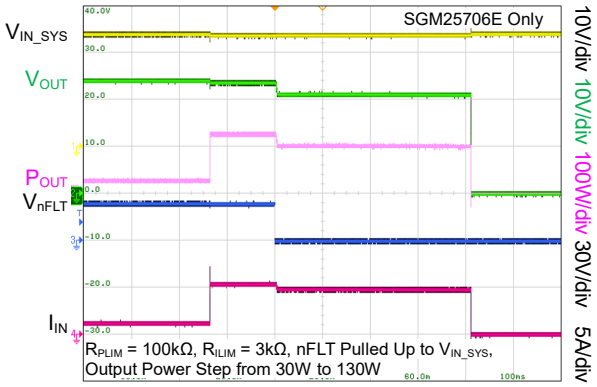
T_A = +25℃, V_{IN_SYS} = 24V, unless otherwise noted.

Output Power Limiting Response



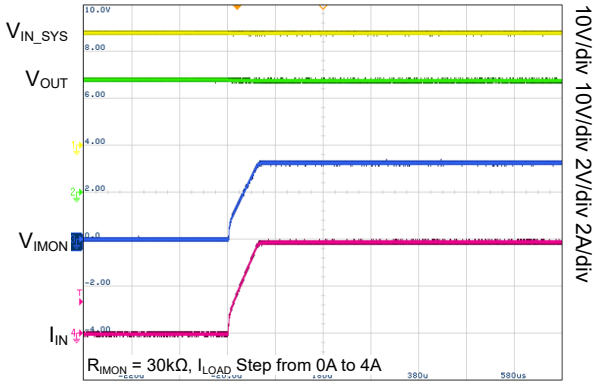
Time (20ms/div)

Output Power Limiting Response



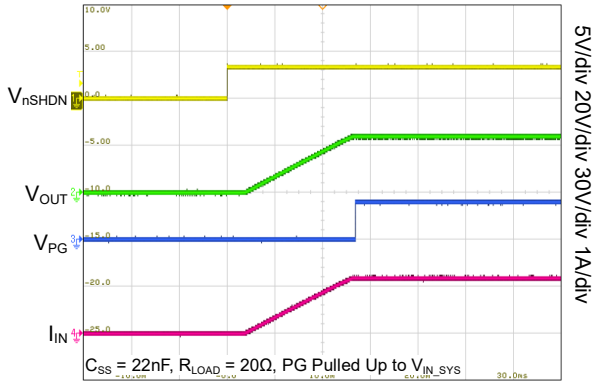
Time (20ms/div)

IMON Response during a Load Step



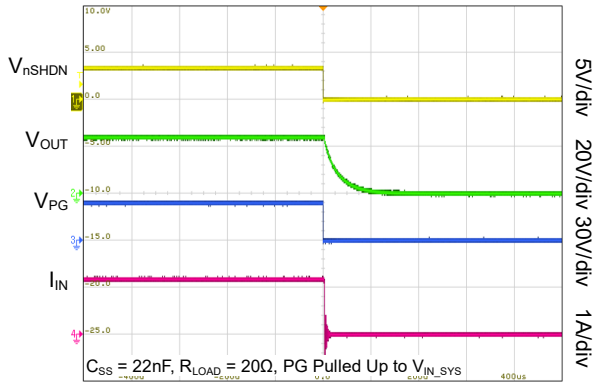
Time (100μs/div)

Turn-On Control with nSHDN



Time (5ms/div)

Turn-Off Control with nSHDN



Time (100μs/div)

FUNCTIONAL BLOCK DIAGRAM

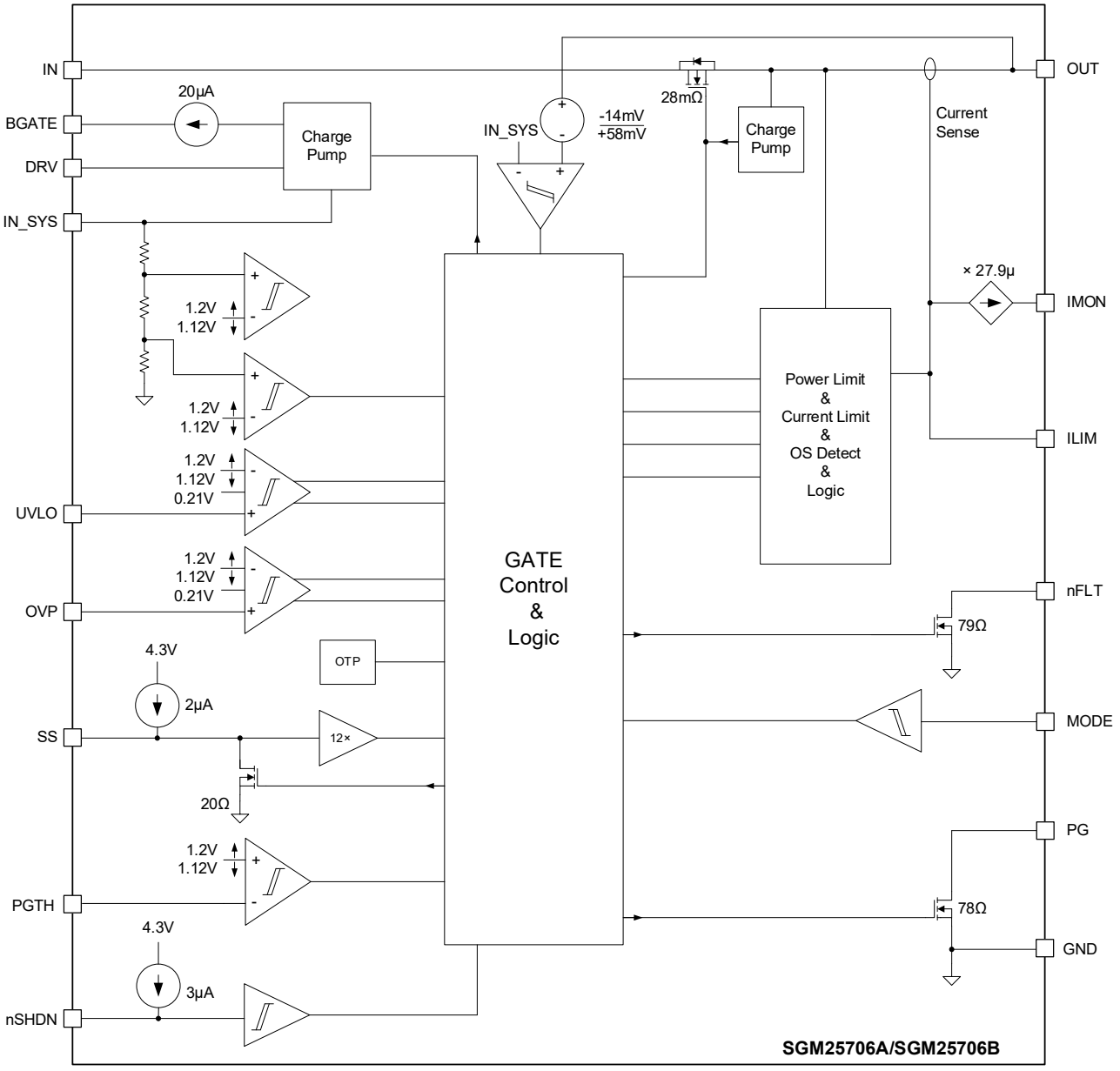


Figure 5. SGM25706A and SGM25706B Block Diagram

FUNCTIONAL BLOCK DIAGRAM (continued)

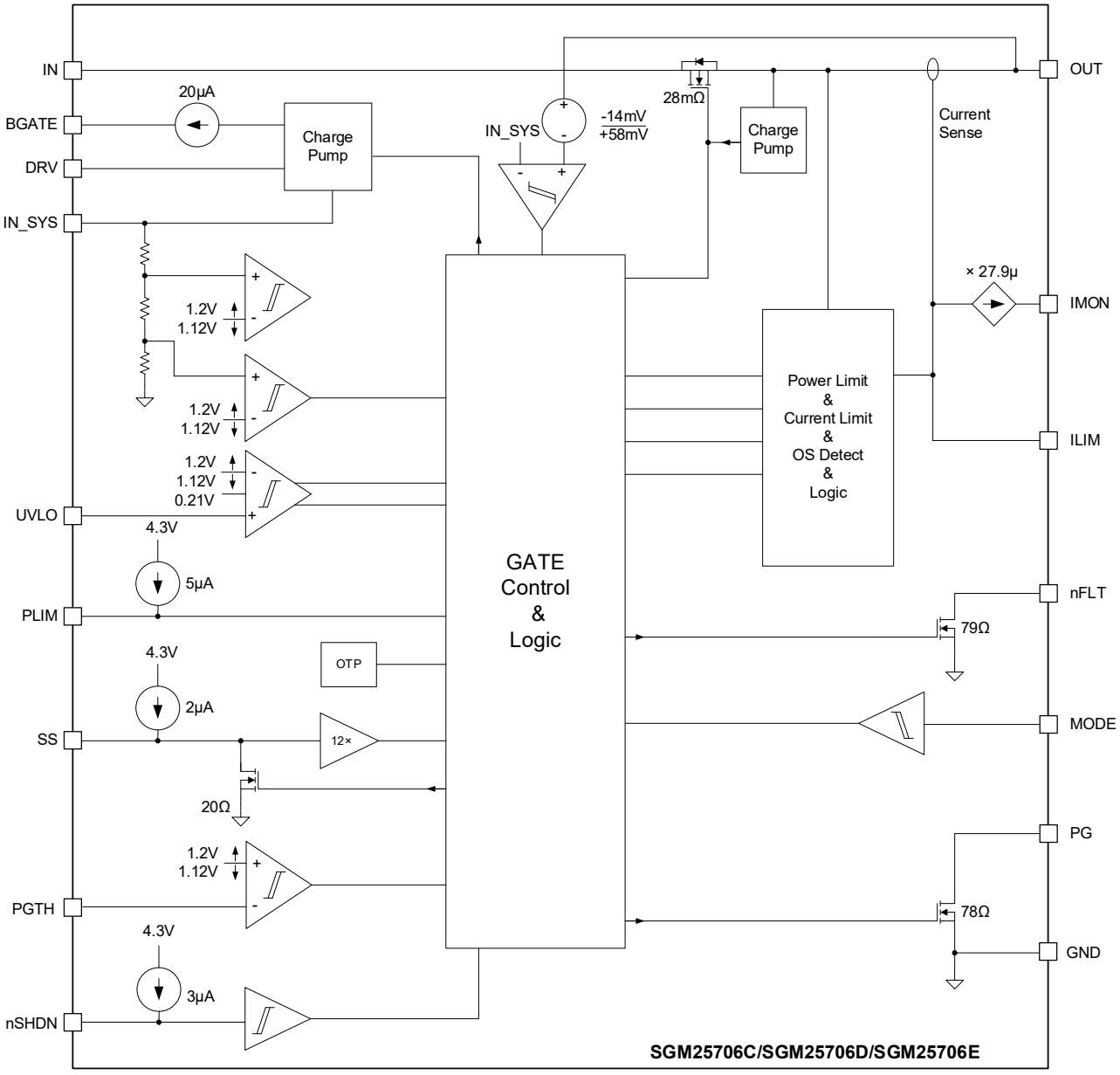


Figure 6. SGM25706C, SGM25706D and SGM25706E Block Diagram

DETAILED DESCRIPTION

Overview

The SGM25706x series of 60V industrial eFuses provide comprehensive protection for various 4.5V to 60V power applications. The devices offer input reverse polarity protection up to -60V through an external N-MOSFET. For hot-plug applications, the devices provide inrush current management and output ramp rate control. Besides, the device offers many other protections such as under-voltage, over-voltage, over-current and reverse current protections. The accurate over-current limit (±8% at 6A) threshold reduces the system over-design. Under output short-circuit condition, the fast-trip short-circuit protection shuts down the device and cuts off the fault current within 0.3μs. The device cuts off the reverse current with a 0.183μs response time. The above features of SGM25706 simplify system designs for surge compliance and device protections.

The SGM25706 can distinguish between real system faults and transient event (such as real input under-voltage and transient input spike) and control the recovery behavior differently. This feature is realized through monitoring the output voltage at the PGTH pin. This ensures fast recovery of the device under tests such as input surge and input brown out tests.

The SGM25706C, SGM25706D and SGM25706E provide programmable output power limiting (PLIM) function which is for applications that demand limited output power.

The SGM25706 offers accurate monitoring of bus voltage and asserts the fault indicator pin (nFLT) under input under-voltage and over-voltage condition without additional voltage supervisor. The part continuously monitors the voltage of IN_SYS (V_{IN_SYS}) and OUT (V_{OUT}) to provide reverse current protection once V_{OUT} - V_{IN_SYS} reaches the detection threshold.

Additional features of the SGM25706 devices include:

- Load current monitor at IMON pin with 4.5% at 6A accuracy.
- Selectable auto-retry or latch-off mode response under over-current limit, output power limit and over-temperature through the MODE pin.
- Power Good (PG) indicator through monitoring voltage at PGTH pin with ±2.8% detection threshold.
- Thermal shutdown response under over-temperature protection.
- Fault indicator (nFLT) with de-glitched report for faults such as input under-voltage and over-voltage.
- Enable and disable control using nSHDN pin for micro-controller.

Hot-Plug In and Inrush Current Control

The SGM25706 is designed to provide hot-plug in power management by controlling the inrush current as well as the output slew rate. This design helps eliminate the voltage drop and avoid undesired power reset. The output ramp rate at power-on is set by the capacitor from the SS pin to GND. If SS pin is left open, the device will start up with the fastest output slew rate (24V (10% to 90%)/418μs). The inrush current can be calculated using Equation 1.

$$I = C \times \frac{dV}{dt} \geq I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}} \quad (1)$$

Where

$$t_{SS} = 20.8 \times 10^3 \times V_{IN} \times C_{SS} \quad (2)$$

For detailed performance, refer to *Hot-Plug In and Inrush Current Control at 24V Input* in TYPICAL PERFORMANCE CHARACTERISTICS.

Thermal Regulation Loop

The average power dissipated on the device during start-up process driving a capacitive load can be calculated using Equation 3.

$$P_{D\_INRUSH} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (3)$$

DETAILED DESCRIPTION (continued)

For system designs that require driving large output capacitors, the operating point could exceed the power dissipation versus time boundary limits shown in *Thermal Shutdown Time vs. Power Dissipation* in TYPICAL PERFORMANCE CHARACTERISTICS. Under this condition, the device junction temperature may exceed the over-temperature threshold and cause thermal shutdown. To avoid thermal shutdown, the thermal regulation loop regulates the device junction temperature at T_{J_REG}, +139 ℃ (TYP) through controlling the in-rush current and thereby limit the power dissipation of the device. Once the thermal regulation works, the internal 2.77s timer starts. The device will be turned off if the output does not fully power up within the time, and the following response (auto-retry or latch-off) depends on the MODE pin configuration shown in DEVICE OPERATIONAL VARIATIONS WITH DIFFERENT MODE CONFIGURATIONS. If the MODE pin is configured to auto-retry, the device will restart after a delay of 1.33s.

The thermal regulation loop is enabled during input power-on, UVLO cycling and nSHDN power-on. The thermal regulation loop is disabled internally when the internal MOSFET's gate is fully enhanced after start-up.

For detailed performance, refer to *Thermal Regulation Loop Response* in TYPICAL PERFORMANCE CHARACTERISTICS.

PG and PGTH

The device provides a Power Good (PG) indicator with open-drain output. It can be used to supervise the downstream load. The threshold of PG is set by connecting a resistor network from OUT to PGTH and to GND. The PG asserts (goes high) when the internal MOSFET of the device is fully turned on and the voltage at PGTH (V_{PGTH}) exceeds the V_{PGTHR}. This pin de-asserts when V_{PGTH} drops below V_{PGTHF}. The PG has a 1.35ms (TYP) de-glitch time at the rising edge and a 1.58μs (TYP) de-glitch time at the falling edge. The rating of PG pin is 60V and it can be connected to IN_SYS or OUT through a resistor.

PGTH as OUT Sensing Input

For typical configuration, the PG threshold is set by connecting a resistor network from OUT to PGTH and to GND. During a system transient fault recovery event (such as recovery from input transient under-voltage or over-voltage), the device chooses different recovery behavior based on the V_{PGTH} information (output recovery with internal fast slew rate or with SS slew rate).

Figure 3 shows the turn-on behavior based on V_{PGTH} information. During the recovery process, if V_{PGTH} is greater than V_{PGTHF}, the internal MOSFET is turned on with the fastest slew rate (ignoring the capacitor at SS pin) after a delay of $t_{OVP\_ON\_FAST\_DLY}$. Meanwhile, the thermal regulation loop is enabled for 2.77s. The maximum current through the device is limited to I_{OL} for SGM25706A and SGM25706C and to 2 × I_{OL} for SGM25706B, SGM25706D and SGM25706E for a duration of t_{CB_DLY}). If V_{PGTH} is lower than V_{PGTHF}, the internal MOSFET is turned on with the slew rate controlled by the SS capacitor. The maximum current through the device is limited to I_{OL}. With this design, the device is able to distinguish between real faults and transient faults and choose different recovery behavior accordingly. This design makes the device recover fast under transient test such as input surge or brown out tests. Besides, this design can be disabled by pulling PGTH to GND, and PG will be constant low level under this case.

Under-Voltage Lockout (UVLO)

The SGM25706 provides programmable under-voltage lockout (UVLO) protection with ±2.8% threshold accuracy. When the voltage of UVLO (V_{UVLO}) drops below the falling threshold V_{UVLOF}, the internal MOSFET is turned-off and nFLT pin is asserted. The UVLO hysteresis is 78mV (TYP). The UVLO threshold can be set through connecting a resistor network from IN_SYS to UVLO pin and to GND. The device has a 15.38V (rising) default UVLO threshold with 0.93V hysteresis which is selected by pulling UVLO pin to GND. If the UVLO protection is not used, the UVLO pin must be connected to IN_SYS and must not be floating. For applications that input reverse polarity protection is needed, place at least a 300kΩ resistor between UVLO and IN_SYS.

Figure 2 shows the turn-on behavior when V_{UVLO} exceeds V_{UVLOR} threshold.

DETAILED DESCRIPTION (continued)

Over-Voltage Protection (OVP)

The SGM25706 series of device provide robust input over-voltage protection. The SGM25706A and SGM25706B offer programmable over-voltage lockout (OVLO) protection with ±2.8% threshold accuracy. When the voltage on OVP pin exceeds the rising threshold V_{OVPR}, the internal MOSFET is turned off. The OVP threshold can be set by connecting a resistor network from IN_SYS to OVP pin and to GND.

The SGM25706A and SGM25706B also provide a default 34.16V OVLO threshold $V_{IN\_SYS\_OVP}$ with 490mV hysteresis which can be enabled by pulling OVP pin to GND.

The SGM25706C and SGM25706D offer a fixed 34.7V (MAX) over-voltage clamp (OVC) protection, while the SGM25706E offers 38.4V (MAX) over-voltage clamp (OVC) protection. During the OVC protection, excess power is dissipated on the device which could increase the device temperature. To suppress the temperature rise, the device has a 170ms maximum duration for OVC operation. After this duration, the internal MOSFET is turned off and the following behavior (auto-retry or latch off) depends on the MODE pin configuration.

Figure 2 illustrates the OVP behavior. For OVLO functionality, the nFLT is asserted with a 2μs (TYP) delay after voltage on OVLO pin exceeds V_{OVPR}. For OVC functionality, the nFLT is asserted with a 691μs (TYP) delay after the device enters OVC operation. For both conditions, the nFLT would remain asserted until the over-voltage fault is removed.

For detailed performance, refer to *Over-Voltage Cut-Off Response at 33V Level* and *Over-Voltage Clamp Response* in TYPICAL PERFORMANCE CHARACTERISTICS.

Input Reverse Polarity Protection (BGATE, DRV)

The SGM25706 provides input reverse polarity protection. Connect an external N-MOSFET (Q1) with the Source terminal to IN_SYS pin, Drain terminal to IN pin, and Gate terminal to BGATE pin as shown in Figure 7. This connection makes the external MOSFET back to back connection with the internal MOSFET of the device and protects the device against input reverse polarity fault. Besides, an external small signal MOSFET (Q2) is needed to quickly pull down the external MOSFET (Q1). Connect its Source terminal to IN_SYS pin, Drain terminal to BGATE pin (Gate terminal of Q1) and Gate terminal to DRV pin. If the input reverse polarity protection is not needed, both Q1 and Q2 are not needed and IN is directly connected to IN_SYS with BGATE and DRV pin floating as shown in Figure 8.

The SGM25706 supports a maximum voltage difference between IN_SYS and OUT, namely V_{IN_SYS} - V_{OUT}, up to -85V. The voltage stress is withstood by the external MOSFET Q1. The device offers a 10.08V gate driving voltage at BGATE pin. The signal MOSFET Q2 pulls down the gate of Q1 under reverse polarity and reverse current faults. Under proper design, Q2 should have a minimum V_{DS} rating of 15V and a maximum V_{GS} rating of 20V. The input capacitance C_{ISS} should be less than 50pF with the turn-on threshold voltage V_{TH} less than 1.5V.

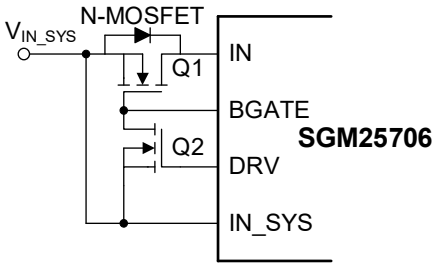


Figure 7. Configuration for Input Reverse Polarity Protection and Reverse Current Blocking

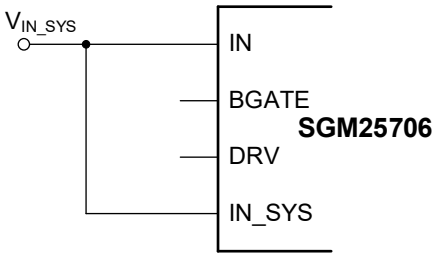


Figure 8. Configuration for Applications without Input Reverse Polarity Protection and Reverse Current Blocking Requirement

DETAILED DESCRIPTION (continued)

Reverse Current Protection

The SGM25706 provides reverse current protection through monitoring the V_{IN_SYS} and V_{OUT}. When V_{IN_SYS} - V_{OUT} drops below -14mV, the reverse protection works and quickly turns off the external MOSFET Q1. The total response time to turn off Q1 is $t_{RCB\_FAST\_DLY}$ + t_{DRIVER} where t_{DRIVER} is the time taken to turn off Q1 which can be calculated using Equation 4.

$$t_{DRIVER} = -R_{DSON\_Q2} \times C_{ISS\_Q1} \times \ln(\frac{V_{TH\_Q1}}{V_{BGATE}}) \quad (4)$$

Where

- R_{DSON_Q2} is the on-resistance of pull-down MOSFET Q2.
- C_{ISS_Q1} is the input capacitance of the blocking MOSFET Q1.
- V_{TH_Q1} is the turn-on threshold voltage of Q1.
- V_{BGATE} = 10.08V (TYP).

For typical design, t_{DRIVER} is generally 10% to 20% of $t_{RCB\_FAST\_DLY}$ of 0.183μs (TYP).

Overload and Short-Circuit Protection

The device monitors the load current continuously to provide over-load protection.

Overload Protection

Set the current limit using Equation 5.

$$I_{OL} = \frac{18}{R_{ILIM}} \quad (5)$$

Where

- I_{OL} is the overload current limit in A.
- R_{ILIM} is the current limit resistor in kΩ.

Active Current Limit at 1 × I_{OL}, (SGM25706A and SGM25706C Only)

For SGM25706A and SGM25706C, the load current is limited to 1 × I_{OL} under over-load condition. The output voltage under regulation decreases which will increase the device power dissipation and cause device temperature rise. To suppress this, the device has a $t_{CL\_PLIM\_DLY}$ (171ms TYP) maximum duration for over-current limit operation. Within this time duration, if the device temperature exceeds the over-temperature threshold, the internal MOSFET is turned off due to thermal shutdown, and the following behavior (auto-retry or latch-off) depends on the MODE pin configuration. If the device continuously operates at over-current manner for this 171ms time, then the internal MOSFET will be turned off after this duration. Likely, the following behavior (auto-retry or latch-off) depends on the MODE pin configuration.

Active Current Limit with 2 × I_{OL} Pulse Current Support, (SGM25706B, SGM25706D and SGM25706E Only)

For SGM25706B, SGM25706D and SGM25706E, after the power-up with V_{PGTH} above V_{PGTHR}, if the load current exceeds I_{OL}, an internal t_{CB_DLY} (26.3ms TYP) timer starts. During this time, the load current allowed to pass through the device will be limited to not more than 2 × I_{OL} (load current more than 2 × I_{OL} will be regulated to 2 × I_{OL}). After t_{CB_DLY} time, the load current is regulated to I_{OL}. The maximum time duration for the 1 × I_{OL} over-current limit operation is $t_{CL\_PLIM\_DLY}$. The following behavior (auto-retry or latch-off) depends on the MODE pin configuration. During the current limit operation, if the device temperature exceeds the over-temperature threshold, the internal MOSFET is turned off due to thermal shutdown, and the following behavior (auto-retry or latch-off) depends on the MODE pin configuration.

The 2 × I_{OL} current limit feature is only activated after V_{PGTH} exceeds V_{PGTHR}. If V_{PGTH} is below V_{PGTHF} during conditions such as power-up or auto-retry, the 2 × I_{OL} current limit function will not be activated and the device will limit current at I_{OL}.

The SGM25706 provides ILIM pin open and short state detection. The internal MOSFET is turned off when ILIM pin is detected in short or open state, and remains turn-off until the fault is removed.

Refer to *Overload Performance, Load Step from 50Ω to 15Ω* and *Response during Coming Out of Overload Fault* in TYPICAL PERFORMANCE CHARACTERISTICS for detailed performance.

DETAILED DESCRIPTION (continued)

Short-Circuit Protection

When the output short-circuit occurs, the current from IN to OUT rises very rapidly. Due to limited bandwidth, the current limit amplifier is unable to respond quickly to this fault. To solve this, the SGM25706 integrates with a fast-trip comparator which can shut down the internal MOSFETs within 0.3μs (TYP) with I_{SCP} = 37A. The fast-trip comparator works and cuts off the short-circuit current when the current through the device I_{OUT} exceeds the fast-trip threshold $I_{FASTRIP}$. The internal MOSFETs would remain OFF state for only a few ms, following by soft-restart in a current limit manner where current through the device is regulated to I_{OL} under the regulation of current limit amplifier. Then, the device behaves the same as the overload condition.

For robust performance, the fast-trip comparator is designed with a line voltage noise immunity. This is achieved by changing the turn-off time of the internal MOSFET with the over-current level. The turn-off time is faster under higher over-current level. The response time of fast-trip comparator is 2μs (TYP) when $I_{FASTTRIP} < I_{OUT} < I_{SCP}$.

Start-Up with Short-Circuit On Output

For power-up with output short-circuit to GND, the current through the device is limited to I_{OL}. Due to high power dissipation of the device (V_{IN} × I_{OL}), the junction temperature of the device increases rapidly. When the temperature reaches the thermal regulation point, the thermal regulation loop works and limits the load current to maintain the device temperature at T_{J_REG}, +130℃ (TYP) for a duration of $t_{TREG\_TIMEOUT}$, 2.77s (TYP). The following behavior (auto-retry or latch-off) depends on the MODE pin configuration. The nFLT is asserted after $t_{TREG\_TIMEOUT}$ and remains asserted until the output short-circuit fault is removed. *Start-Up with Short on Output* in TYPICAL PERFORMANCE CHARACTERISTICS shows the device performance under power-on with output short-circuit.

Output Power Limiting, PLIM (SGM25706C, SGM25706D and SGM25706E Only)

For SGM25706A and SGM25706B, the output power is limited to V_{OUT} × I_{OL} which increases linearly with the input supply voltage. For applications that require limiting the output power under wide input voltage range, this design is difficult to achieve. To solve this, the SGM25706C, SGM25706D and SGM25706E provide programmable output power limiting functionality. The output power limit level is set by placing a resistor from PLIM pin to GND. If the output power limiting is not used, tie the PLIM pin to GND directly.

For SGM25706C, the device limits the output power at the level set by the PLIM resistor under output over-power condition. The output power limit functionality indirectly results in the device operation in current limit mode with P_{LIM} = V_{OUT} × I_{OUT}. *I_{PLIM}, P_{PLIM} vs. V_{IN_SYS}* in TYPICAL PERFORMANCE CHARACTERISTICS shows the device behavior under 110W power limit level. The device has a 171ms $t_{CL\_PLIM\_DLY}$ maximum time duration for output power limiting operation. After this time, the device behavior (auto-retry or latch-off) depends on the MODE pin configuration.

For SGM25706D and SGM25706E, the output power is limited to V_{OUT} × 2 × I_{OL} for a maximum duration of t_{CB_DLY}, 26.3ms (TYP). After this duration, the output power is limited to PLIM set by the PLIM resistor. The power limit is set using Equation 6.

$$P_{PLIM} = R_{PLIM}^{1.04} - 9 \quad (6)$$

Where P_{PLIM} is output power limit in W, R_{PLIM} is the power limit setting resistor in kΩ.

For detailed performance, refer to *Output Power Limiting Response* in TYPICAL PERFORMANCE CHARACTERISTICS.

DETAILED DESCRIPTION (continued)

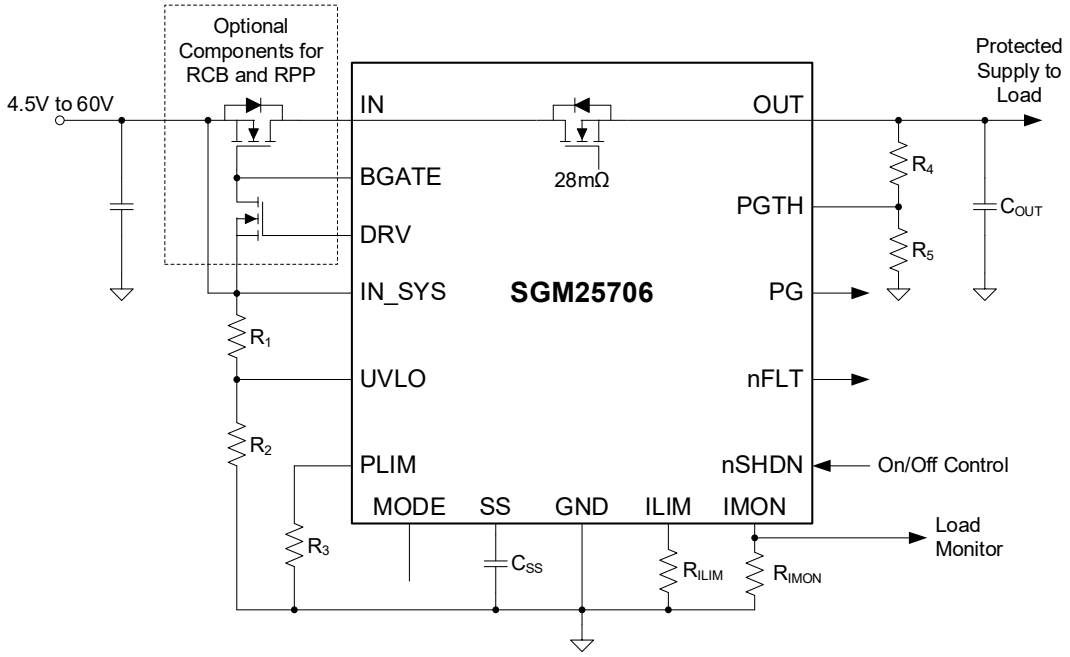


Figure 9. SGM25706C/D/E Typical Application Schematic

Current Monitoring Output (IMON)

The SGM25706 has a current monitoring function at the IMON pin. The sourcing current of this pin is proportional to the current of internal MOSFETs. By placing a resistor R_{IMON} from this pin to GND, this monitored current is converted to IMON voltage.

The maximum voltage on the IMON pin is internally limited to 4V. With this limitation, the maximum value of R_{IMON} can be determined using Equation 7.

$$V_{IMON} = \left[I_{OUT} \times GAIN_{IMON}\right] \times R_{IMON} \quad (7)$$

Where

- $GAIN_{IMON}$ is the gain factor I_{IMON} : I_{OUT} = 27.9μA/A (TYP).
- I_{OUT} is the load current.

Please do not place bypass capacitor at IMON pin which could cause delay in current monitoring.

For detailed performance, refer to *IMON Response during a Load Step* in TYPICAL PERFORMANCE CHARACTERISTICS.

FAULT Response (nFLT)

The SGM25706 has an open-drain fault indicator nFLT pin which asserts under input under-voltage, input over-voltage, current limiting, output power limiting, reverse current, ILIM pin open or short and thermal shutdown. To avoid false reporting, this pin is designed with an internal de-glitch without additional external circuits. The nFLT pin can be left open or tied to GND if not used.

IN_SYS, IN, OUT and GND Pins

Place a minimum of 0.1μF bypass capacitor from IN_SYS pin to GND.

For system that requires reverse current protection or input reverse polarity protection:

Connect an external N-MOSFET with Source terminal connected to IN_SYS, Drain terminal to IN, and Gate terminal to BGATE.

Connect an external signal MOSFET with Source terminal to IN_SYS, Drain terminal to BGATE and Gate terminal to DRV.

If the reverse current protection and reverse polarity protection are not used, connect IN_SYS to IN directly, and the BGATE and DRV pin can be left open.

DETAILED DESCRIPTION (continued)

Thermal Shutdown

The SGM25706 incorporates over-temperature protection with thermal shutdown function. The internal MOSFETs will be turned off when the junction temperature T_J exceeds T_{SD} (+167℃ TYP). After that, the device will remain latched-off or auto-retry with a delay of 682ms (TYP), t_{TSD_RETRY} after $T_J < (T_{SD} - 16℃)$ depending on the MODE pin configuration. During thermal shutdown, the nFLT pin is asserted.

Low Current Shutdown Control (nSHDN)

The device can be shut down through pulling the nSHDN pin below the 0.8V (TYP) threshold with a micro-controller. In shutdown mode, the quiescent current of the device is reduced to 19μA (TYP). The controller or any other device should have at least 8μA sinking current capability to pull down the nSHDN pin. To enable the device, nSHDN should be pulled up to at least 1.8V where the device starts up with soft-start mode.

APPLICATION INFORMATION

Typical Application

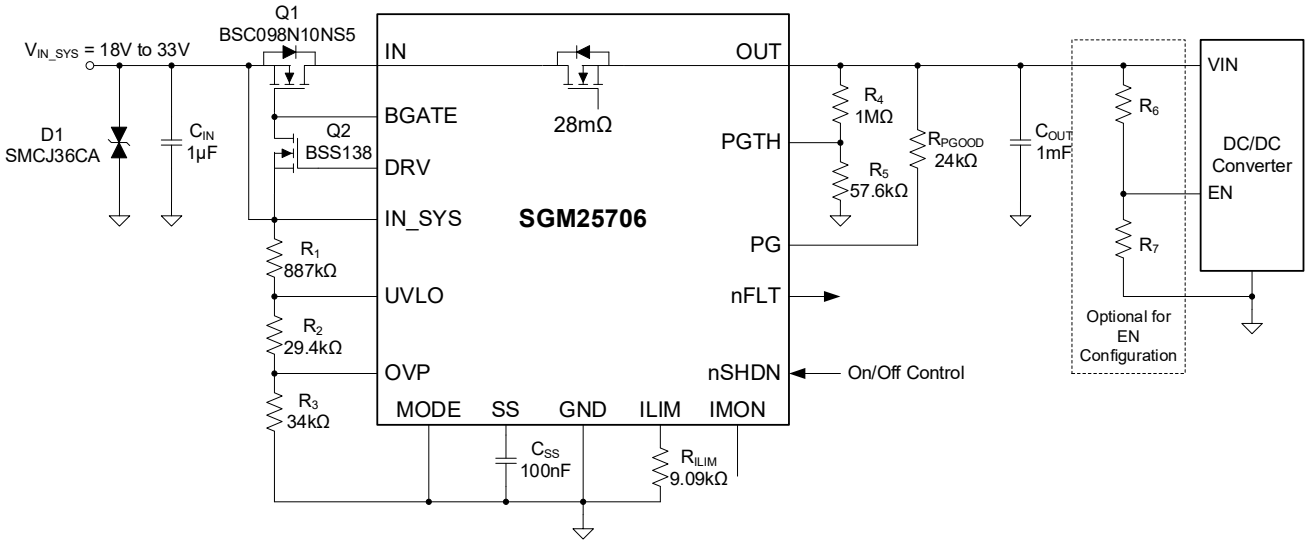


Figure 10. Typical Application Schematics: 24V, 2A eFuse Input Protection Circuit

Design Requirements

Table 1 shows the Design Requirements for SGM25706.

Table 1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
V_{IN}	Typical Input Voltage	24V
V_{UV}	Under-Voltage Lockout Set Point	18V
V_{OV}	Over-Voltage Cutoff Set Point	33V
V_{PG}	Output Power Good Threshold	22V
I_{LIM}	Overload Current Limit	2A
I_{INRUSH}	Inrush Current Limit	500mA
P_{OUT}	Output Load	15W (DC-DC) with 15V $V_{IN\_MIN\_DC\text{-}DC}$
t_{FAIL_TR}	Power Interruption Time	10ms

Detailed Design Procedure

Programming the Current-Limit Threshold: R_{ILIM} Selection

The current limit level is set by the ILIM pin resistor R_{ILIM} which can be calculated using Equation 8.

$$R_{ILIM} = \frac{18}{I_{OL}} = 9k\Omega \quad (8)$$

Where

- I_{LIM} = 2A.

Choose the closest standard 1% resistor value: R_{ILIM} = 9.09kΩ

Under-Voltage Lockout and Over-Voltage Set Point

The UVLO and OVLO threshold value are set through a resistor network of R_1, R_2 and R_3 connected between IN_SYS pin, UVLO pin, OVP pin and GND pin. These resistors are selected based on Equation 9 and 10.

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \quad (9)$$

$$V_{UVLOR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \quad (10)$$

To reduce the current drawn from the power supply, resistors with higher value for R_1 to R_3 are recommended.

However, using higher value resistors may introduce more calculation errors affected by the leakage current into the device pins. Therefore, the current through the resistor $V_{IN\_SYS}/(R_1 + R_2 + R_3)$ should be 20 times greater than the leakage current into the UVLO and OVP pins.

Form the electrical specifications, V_{OVPR} = 1.2V and V_{UVLOR} = 1.2V. For this design, V_{OV} is 33V and V_{UV} is 18V. First, choose R_3 = 34kΩ first, and use Equation 9 to solve (R_1 + R_2) = 916kΩ. Combine this with Equation 10 to solve R_2 = 29.4kΩ and R_1 = 887kΩ.

Choose the closest standard 1% resistor values: R_1 = 887kΩ, R_2 = 29.4kΩ and R_3 = 34kΩ.

APPLICATION INFORMATION (continued)

Output Capacitor: C_{OUT}

During the power failure time, the output capacitor C_{OUT} delivers energy to the downstream 15W converter load. The required capacitor C_{OUT} is calculated using Equation 11.

$$C_{OUT} = \frac{2 \times P_{DC-DC} \times t_{FAIL\_TR}}{V_{IN\_SYS}^2 - V_{UV\_DC-DC}^2} \quad (11)$$

Where

- P_{DC-DC} = 15W/η. Assuming efficiency of 95%, P_{DC-DC} = 15.8W.
- t_{FAIL_TR} = 10ms.
- V_{IN_SYS} = 24V.
- V_{UV_DC-DC} = 15V.

Based on Equation 11, C_{OUT} is 900μF. With ±10% tolerance, a 1mF/35V electrolytic capacitor is selected. Figure 12 shows the performance during the power interruption tests on SGM25706A.

Setting Power Good Assertion Threshold

The power good assertion threshold is set by a resistor divider connected to the PGTH pin. This threshold can be calculated from Equation 12:

$$V_{PG} = \frac{V_{PGTH\_R} \times (R_4 + R_5)}{R_5} \quad (12)$$

Since R_4 & R_5 draw additional current from output, their values need to be taken into account for the acceptable leakage current of the system. The leakage current flowing through R_4 & R_5 from the supply is I_{R45} = $V_{OUT}/(R_4 + R_5)$. Considering that an external active device connected to a resistor divider causes additional leakage current, this increases the calculation error of the supply over-voltage threshold. Therefore, the leakage current flowing through R_4 & R_5 (I_{R45}) should be greater than 20 times the leakage current expected by the PGTH pin.

As can be seen from the ELECTRICAL CHARACTERISTICS, the maximum leakage current of the PGTH pin is 0.15μA, and V_{PGTH_R} = 1.2V. According to the application scenario requirements, V_{PG} = 22V. Given R_4 = 1MΩ, R_5 = 57.6kΩ can be obtained according to the above equation.

Choose the nearest standard 1% resistor values, R_4 = 1MΩ & R_5 = 57.6kΩ are selected.

Setting Output Voltage Ramp Time: (t_{SS})

Based on Equation 1 and Equation 2, the required SS capacitor with an inrush current of 500mA is 0.1μF. Figure 11 illustrates the soft-start and inrush current control performance under 24V hot-plug in power-on.

Support Component Selections - R_{PG} and C_{IN}

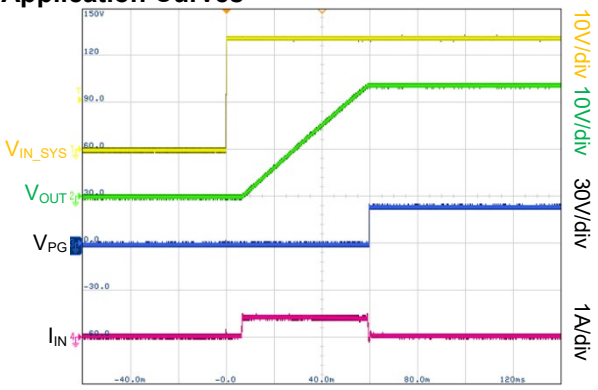
The R_{PG} is used to pull up the open-drain PG. The sink current of this pin must not exceed 10mA (refer to the ABSOLUTE MAXIMUM RATINGS). For typical applications, choose RPOOD in the range of 10kΩ to 100kΩ. C_{IN} is the input bypass capacitor for noise suppression. The minimum recommended value is 1μF.

Selecting Q1, Q2 and TVS Clamp for Surge Protection

For surge test, the SMC sized TVS diode such as SMCJ36CA clamps the surge voltage at around ±55V. Under negative surge, the input voltage VIN_SYS is -55V, and therefore the voltage stress on the external blocking MOSFET Q1 is 55V + 24V = 79V. Choose at least an 80V rated N-MOSFET. The gate driving voltage of Q1 is 10.2V (TYP). Choose MOSFET with proper on-state resistance within this gate voltage. The fast pull-down MOSFET Q2 should be at least 15V rated. The maximum VGS voltage should be 20V with C_{ISS} ≤ 50pF and turn-on threshold voltage V_{TH} ≤ 1.5V. Based on above requirements, the 100V rated BSC098N10NS5 and the 50V rated BSS138 are chosen for Q1 and Q2 respectively.

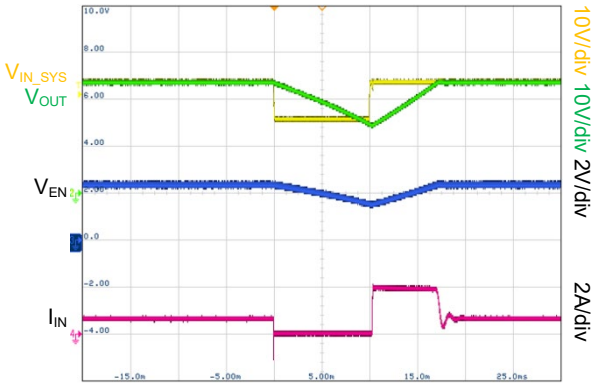
APPLICATION INFORMATION (continued)

Application Curves



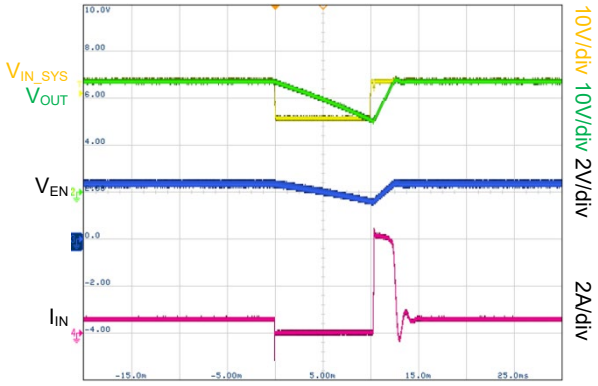
Time (20ms/div)

Figure 11. Hot-Plug In at 24V Supply



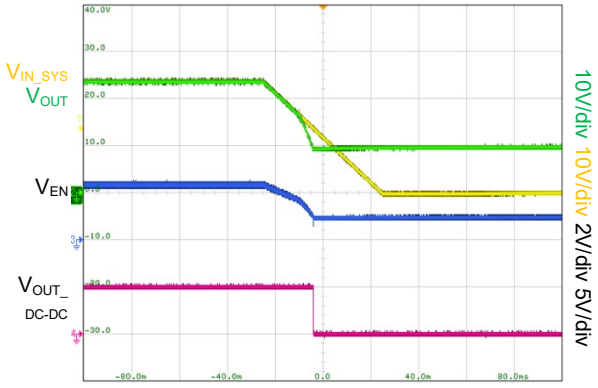
Time (5ms/div)

Figure 12. Voltage Interruption Response with SGM25706A



Time (5ms/div)

Figure 13. Voltage Interruption Response with SGM25706B



Time (20ms/div)

Figure 14. Power Down Response

APPLICATION INFORMATION (continued)

System Example

Simple 24V Power Supply Path Protection

For SGM25706, a simple power supply protection scheme is available with a minimum of five external components as shown in Figure 15. The required external components are: an N-MOSFET Q1, a fast pull-down N-MOSFET Q2 and a current limit resistor R_{ILIM}, C_{IN} and C_{OUT} capacitors.

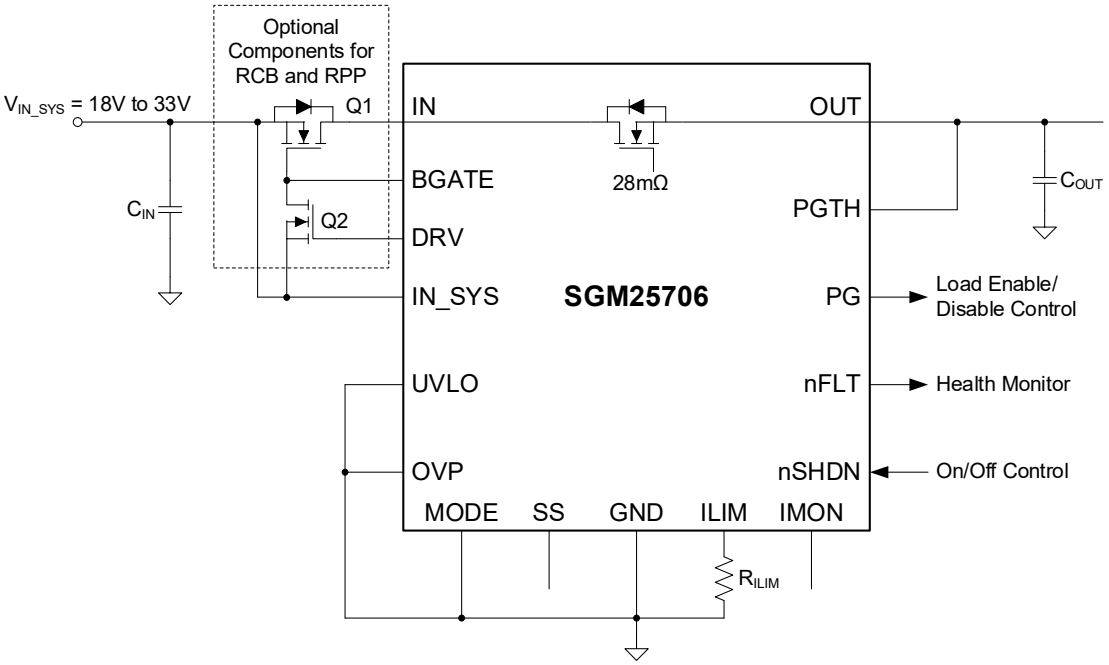


Figure 15. SGM25706A Configured for a Simple 24V Supply Path Protection

This configuration provides protections include:

- Input reverse polarity fault protection.
- Input over-voltage cut-off protection.
- Inrush current control with default 24V (10% to 90%)/418μs output voltage slew rate.
- Reverse current blocking.
- Precise current limiting.

Power Supply Recommendations

The SGM25706 is designed to operate with 4.5V to 60V input voltage range. For input supply located more than a few inches from the IN_SYS terminal, it is recommended to place a bypass capacitor with more than 0.1μF.

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input with a negative voltage spike occuring at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the OUT pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

The value of the input capacitance can be calculated from the Equation 13:

$$V_{SPIKE\_ABSOLUTE} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (13)$$

Where V_{IN} is the rating of the input voltage, I_{LOAD} is the load current, L_{IN} is the effective inductance seen looking into the source, and C_{IN} is the capacitance of the input.

APPLICATION INFORMATION (continued)

For applications such as USB-C interfaces, the power cord may be plugged into the output of the device. In this case, the voltage stress from OUT to IN may exceed the absolute maximum rating, so it is recommended to add a TVS diode from OUT to IN to clamp the voltage for safety.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 16.

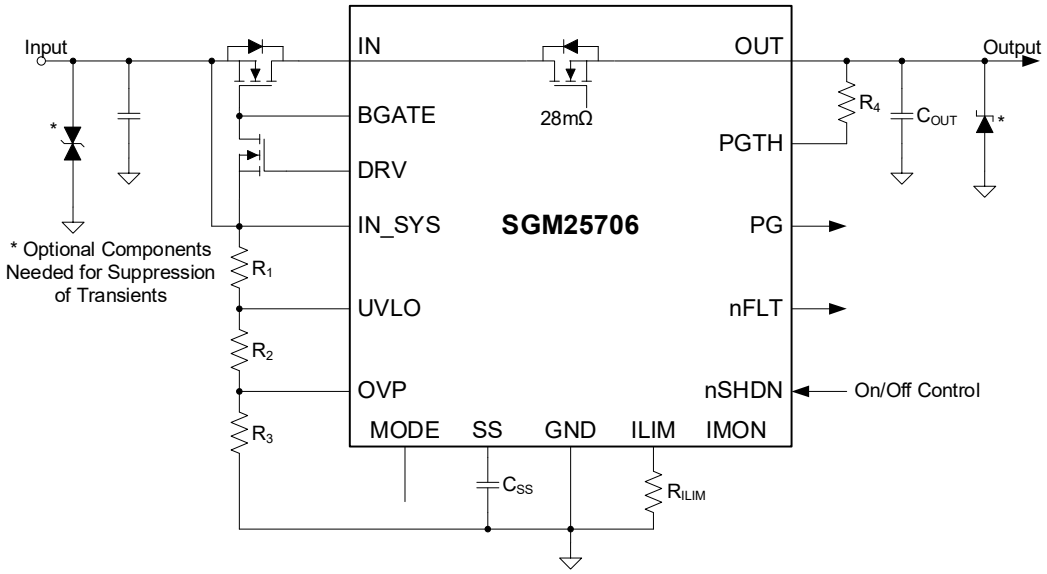


Figure 16. Circuit Implementation with Optional Protection Components

Layout Guidelines

In any application, it is recommended to connect a decoupling capacitor of 0.1μF or greater between IN_SYS and GND. This decoupling capacitor should be as close as possible to IN_SYS and GND pins.

The external MOSFET Q1 should be placed with its Drain terminal close to the IN pin of the device through plane. The fast pull-down MOSFET Q2 should be placed with its Drain terminal close to the Gate terminal of Q1, and Source terminal close to the Source terminal of Q2.

The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.

The GND pin of the device must be connected to PCB ground which is a copper plane or island as short as possible.

The IN and OUT pins of the device are used to dissipate heat. Therefore, these two pins should be dissipated as much as possible through the copper plane on the top layer or bottom layer on the PCB. Placing thermal vias on the copper plane improves on-resistance as well as current sensing accuracy.

External components of the device as follows should be placed as close to the corresponding pins as possible:

- R_{ILIM}
- C_{SS}
- Resistor dividers of IMON, UVLO, OVP and PGTH

The other end of these components is connected to ground via the shortest possible path. The ILIM pin should have a parasitic capacitance of less than 50pF, and the connection path of this pin should be away from the switching signal.

Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.

Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.

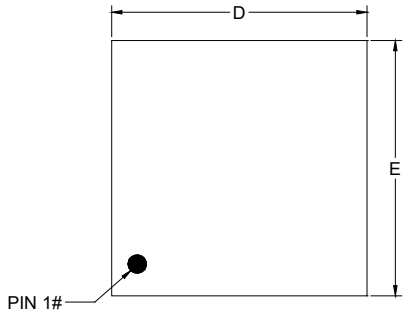
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

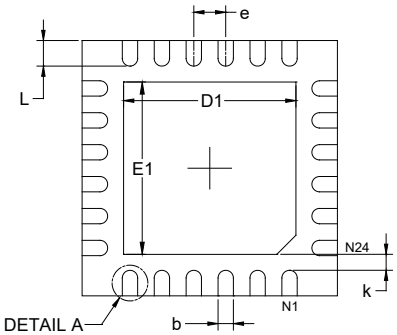
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

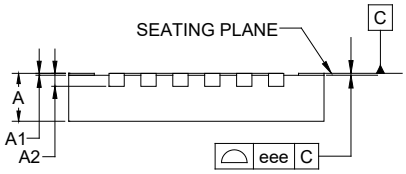
TQFN-4×4-24L



TOP VIEW

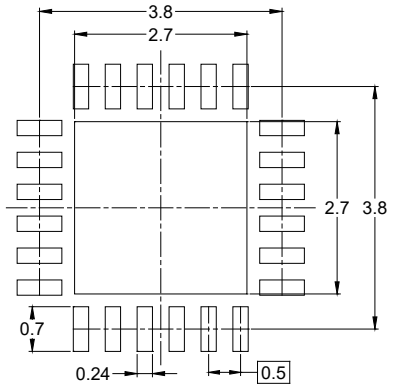


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



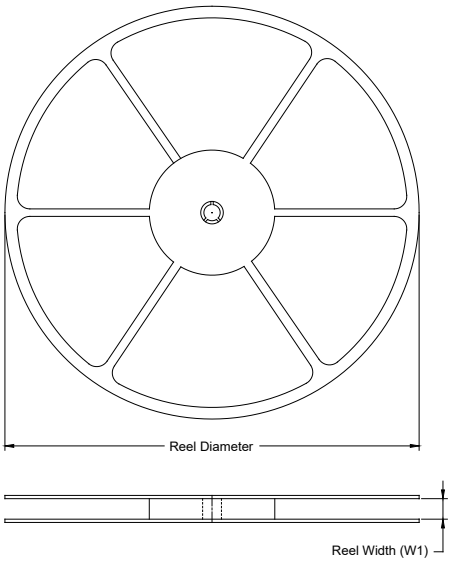
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e		0.500 BSC	
k		0.200 MIN	
L	0.300	-	0.500
eee		0.080	

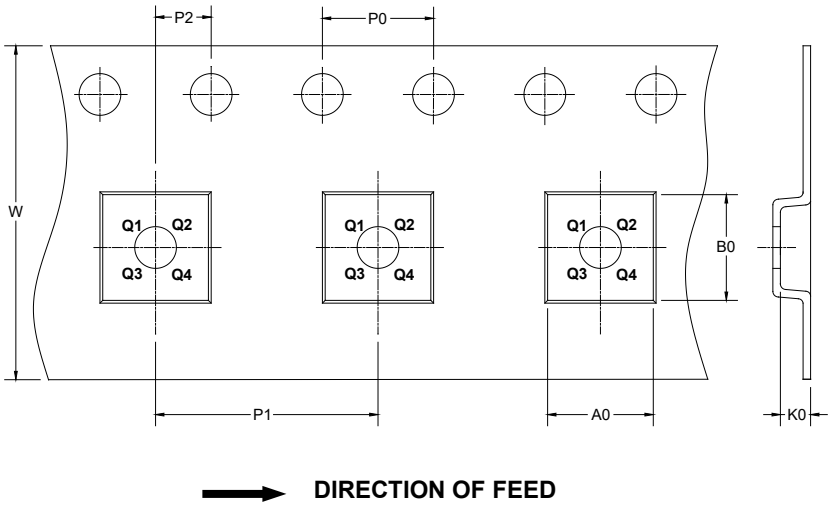
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



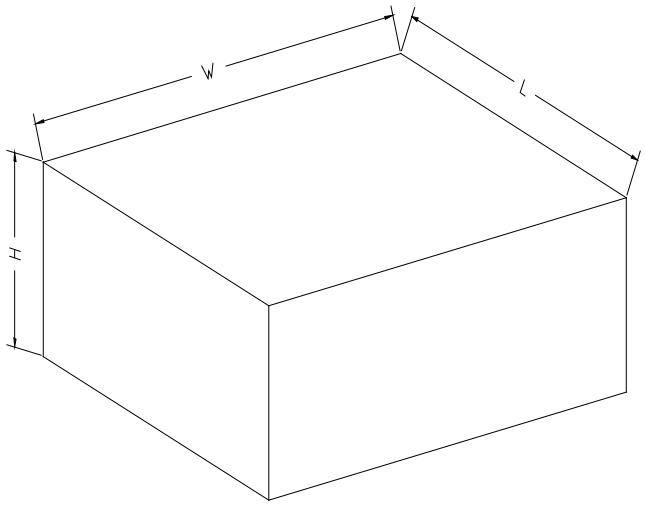
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002