SGM2069
1.5A, High PSRR, Low Dropout Linear Regulator with Programmable Soft-Start

GENERAL DESCRIPTION

The SGM2069 is a high PSRR and low dropout linear regulator with programmable soft-start. It is capable of supplying 1.5A output current with typical V_{IN} dropout voltage of only 110mV. The operating input voltage range is from 0.8V to 5.5V and bias supply voltage range is from 2.7V to 5.5V. The output voltage range is from 0.8V to 3.6V.

Other features include an open-drain power-good (PG) output, logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2069 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2069 is available in Green TQFN-5×5-20L and TDFN-3×3-10AL packages. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **Input Supply Voltage Range: 0.8V to 5.5V**
- **Bias Supply Voltage Range: 2.7V to 5.5V**
- **Adjustable Output from 0.8V to 3.6V**
- **Output Voltage Accuracy: ±1% at +25℃**
- **1.5A Output Current**
- **Quiescent Current: 0.9mA (TYP)**
- **V_{IN} Dropout Voltage: 110mV (TYP) at 1.5A**
- **V_{BIAS} Dropout Voltage: 1200mV (TYP) at 1.5A**
- **Low Noise: 29μV_{RMS} (TYP)**
- **Shutdown Ground Current: 0.1μA (TYP)**
- **Current Limiting and Thermal Protection**
- **Programmable Soft-Start Output**
- **Support Power-Good Indicator Function**
- **With Output Automatic Discharge**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TQFN-5×5-20L and TDFN-3×3-10AL Packages**

APPLICATIONS

Servers
Power for Processors
Power Modules
Consumer Electronics
Programmable Soft-Start Applications

TYPICAL APPLICATION

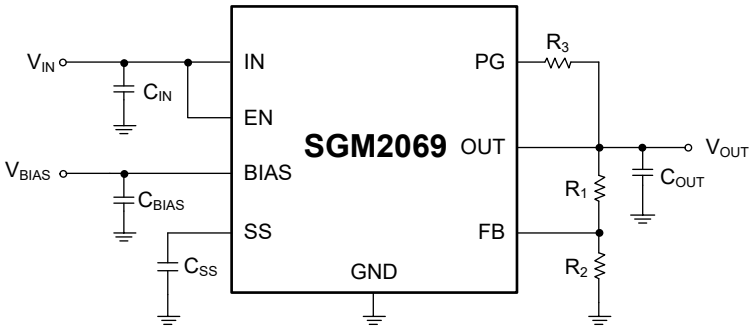


Figure 1. Typical Application Circuit

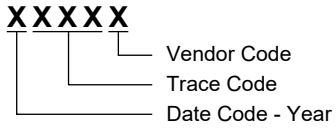
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2069	TQFN-5×5-20L	-40℃ to +125℃	SGM2069XTRM20G/TR	SGM2069 XTRM20 XXXXX	Tape and Reel, 3000
	TDFN-3×3-10AL	-40℃ to +125℃	SGM2069XTGZ10G/TR	SGM 2069GZ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

TQFN-5×5-20L/TDFN-3×3-10AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, BIAS, PG, EN to GND ..... -0.3V to 6V
OUT to GND ..... -0.3V to (V_{IN} + 0.3V)
SS, FB to GND ..... -0.3V to 6V
PG Sink Current, I_{PG} ..... 0mA to 1.5mA
Package Thermal Resistance
TQFN-5×5-20L, θ_{JA} ..... 31.3℃/W
TQFN-5×5-20L, θ_{JB} ..... 12.8℃/W
TQFN-5×5-20L, $\theta_{JC(TOP)}$ ..... 26.1℃/W
TQFN-5×5-20L, $\theta_{JC(BOT)}$ ..... 5.1℃/W
TDFN-3×3-10AL, θ_{JA} ..... 43.9℃/W
TDFN-3×3-10AL, θ_{JB} ..... 17.1℃/W
TDFN-3×3-10AL, $\theta_{JC(TOP)}$ ..... 46.7℃/W
TDFN-3×3-10AL, $\theta_{JC(BOT)}$ ..... 5.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range ..... 0.8V to 5.5V
BIAS Supply Voltage Range ..... 2.7V to 5.5V
Enable Input Voltage Range ..... 0V to 5.5V
Input Effective Capacitance, C_{IN} ..... 1μF (MIN)
BIAS Effective Capacitance, C_{BIAS} ..... 0.1μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 1μF to 1000μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

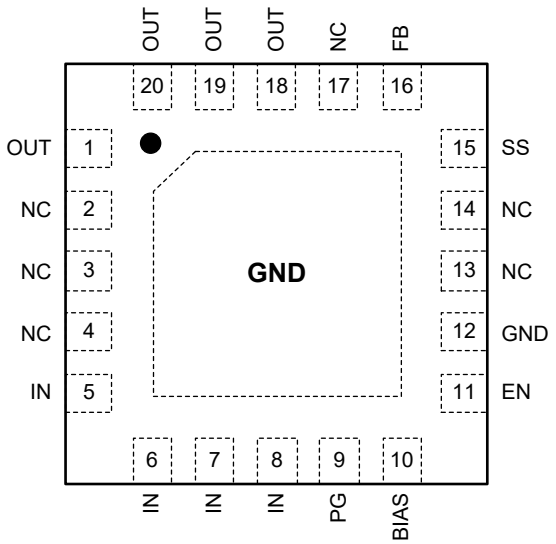
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

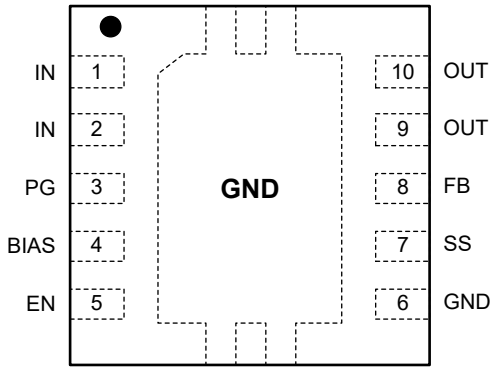
PIN CONFIGURATIONS

SGM2069 (TOP VIEW)



TQFN-5×5-20L

SGM2069 (TOP VIEW)



TDFN-3×3-10AL

PIN DESCRIPTION

PIN		NAME	FUNCTION
TDFN-3×3-10AL	TQFN-5×5-20L		
1, 2	5-8	IN	Input Supply Voltage Pin. It is recommended to use a 2.2μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
3	9	PG	Open-Drain Power-Good Output Pin. An open-drain output and active high when the output voltage reaches the target voltage.
4	10	BIAS	Bias Voltage Supply Pin for Internal Control Circuits. It is recommended to use a 0.22μF or larger ceramic capacitor from BIAS pin to ground and this ceramic capacitor should be placed as close as possible to BIAS pin.
5	11	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
6	12	GND	Ground
7	15	SS	Soft-Start Pin. The soft-start time is determined by an external capacitor connected to this pin.
8	16	FB	Feedback Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
9, 10	1, 18, 19, 20	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 1000μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
—	2, 3, 4, 13, 14, 17	NC	No Connection.
Exposed Pad	Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAM

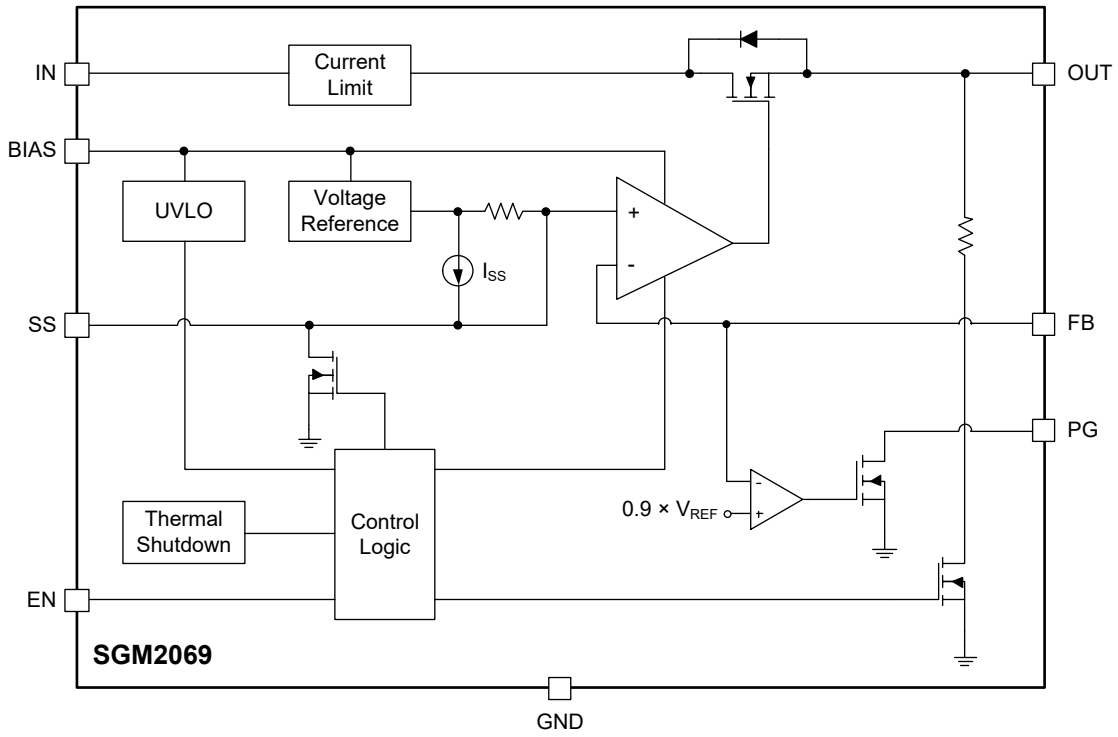


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

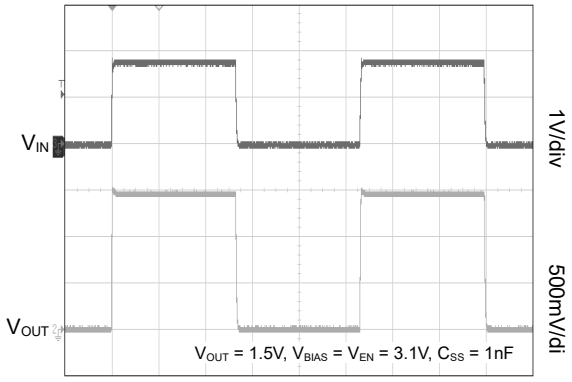
(V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 2.7V or ($V_{OUT(NOM)}$ + 1.6V) whichever is greater, V_{OUT} = 0.8V, V_{EN} = 1.1V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{BIAS} = 0.22μF, C_{OUT} = 10μF, C_{SS} = 1nF, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{IN}			0.8		5.5	V
Bias Supply Voltage Range	V_{BIAS}			2.7		5.5	V
Under-Voltage Lockout	V_{UVLO}	V_{BIAS} rising			1.66	2.10	V
		Hysteresis			138		mV
Feedback Voltage	V_{ADJ}	V_{OUT} = V_{ADJ}, V_{BIAS} = 2.7V to 5.5V, I_{OUT} = 1mA to 1.5A	T_J = +25℃	0.7920	0.8	0.8080	V
			T_J = -40℃ to +125℃	0.7880	0.8	0.8096	
Feedback Pin Current	I_{ADJ}	V_{ADJ} = 0.9V			1	30	nA
IN Pin Current	I_{IN}	I_{OUT} = 0mA			0.11	0.2	mA
BIAS Pin Operating Current	I_{BIAS}	I_{OUT} = 0mA			0.9	1.3	mA
V_{IN} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 5.5V			0.008	0.10	%/V
V_{BIAS} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{BIAS} \times V_{OUT}}$	V_{BIAS} = 2.7V or ($V_{OUT(NOM)}$ + 1.6V) to 5.5V			0.015	0.10	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta I_{OUT}}$	I_{OUT} = 1mA to 1.5A			0.02	0.2	%/A
V_{IN} Dropout Voltage	V_{DROP_IN}	V_{OUT} = 90% × $V_{OUT(NOM)}$, I_{OUT} = 1.5A			110	240	mV
V_{BIAS} Dropout Voltage	V_{DROP_BIAS}	V_{OUT} = 90% × $V_{OUT(NOM)}$, I_{OUT} = 1.5A, V_{IN} = V_{BIAS}			1200	1500	mV
Output Current Limit	I_{LIMIT}	V_{IN} = $V_{OUT(NOM)}$ + 0.6V, V_{OUT} = 97% × $V_{OUT(NOM)}$		1.52	2.6	3.9	A
Short Current Limit	I_{SHORT}	V_{OUT} = 0V			0.95		A
Shutdown Ground Current	I_{SHDN}	V_{EN} ≤ 0.4V	T_J = +25℃		0.1	2	μA
			T_J = -40℃ to +125℃			8	
Enable Threshold Voltage	V_{IH}	EN input voltage high, V_{BIAS} = 2.7V to 5.5V		1		5.5	V
	V_{IL}	EN input voltage low, V_{BIAS} = 2.7V to 5.5V		0		0.4	V
Enable Pin Hysteresis	$V_{EN(HYS)}$				116		mV
Enable Pin Deglitch Time	$V_{EN(DG)}$				27		μs
Enable Pin Current	I_{EN}	V_{EN} = 5.5V			10	1000	nA
Output Discharge Resistance	R_{DIS}	V_{BIAS} = 2.7V		500	770	1200	Ω
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 90% × $V_{OUT(NOM)}$, C_{SS} = open			230		μs
PG High Threshold	PG_{HTH}	V_{OUT} increasing		90	94	98	%V_{OUT}
PG Low Threshold	PG_{LTH}	V_{OUT} decreasing		86	90	94	%V_{OUT}
PG Trip Hysteresis	PG_{HYS}				5		%V_{OUT}
PG Pin Low-Level Output Voltage	$V_{PG(LO)}$	V_{OUT} < V_{IT}, I_{SINK} = 1mA				200	mV
PG Pin Leakage Current	$I_{PG(LKG)}$	V_{OUT} > V_{IT}, V_{PG} = 5.5V			10	500	nA
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.4V			390	650	nA
V_{IN} Power Supply Rejection Ratio	PSRR	V_{IN} to V_{OUT}, V_{OUT} = 1.5V, V_{IN} = 2V, ΔV_{RIPPLE} = 0.2V_{P-P}, I_{OUT} = 1.5A	f = 1kHz		71		dB
			f = 300kHz		36		dB
V_{BIAS} Power Supply Rejection Ratio		V_{BIAS} to V_{OUT}, V_{OUT} = 1.5V, V_{IN} = 2V, ΔV_{RIPPLE} = 0.2V_{P-P}, I_{OUT} = 1.5A	f = 1kHz		61		dB
			f = 300kHz		49		dB
Output Noise Voltage	e_n	V_{OUT} = 1.5V, I_{OUT} = 1.5A, C_{SS} = 1nF, f = 10Hz to 100kHz			29		μV_{RMS}
Thermal Shutdown Temperature	T_{SHDN}				165		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				25		

TYPICAL PERFORMANCE CHARACTERISTICS

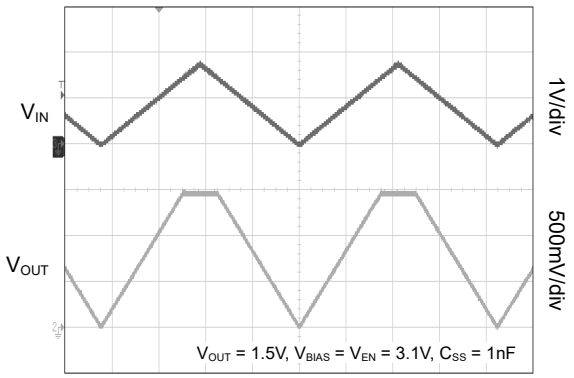
T_J = +25℃, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 2.7V or (V_{OUT} + 1.6V), V_{EN} = V_{BIAS}, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 4.7μF, C_{OUT} = 10μF, unless otherwise noted.

V_{IN} Power-Up/Power-Down Output Waveform



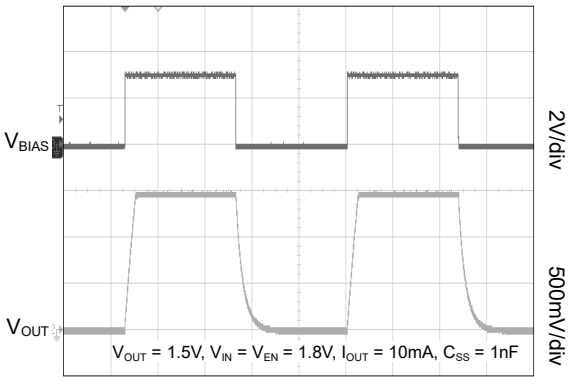
Time (2ms/div)

V_{IN} Power Ramp-Up/Ramp-Down Output Waveform



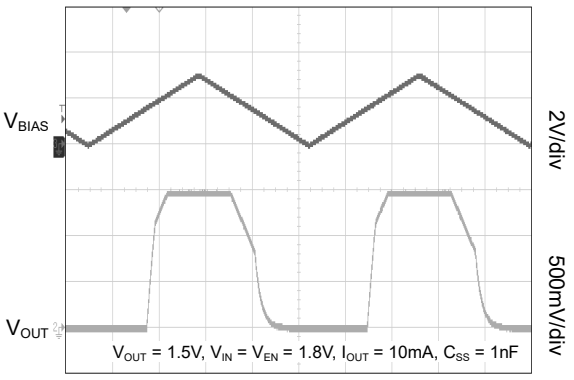
Time (2ms/div)

V_{BIAS} Power-Up/Power-Down Output Waveform



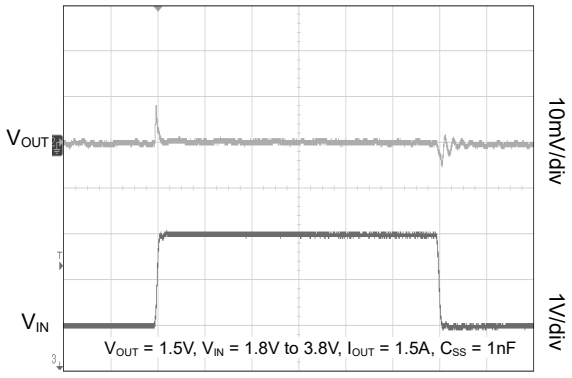
Time (10ms/div)

V_{BIAS} Power Ramp-Up/Ramp-Down Output Waveform



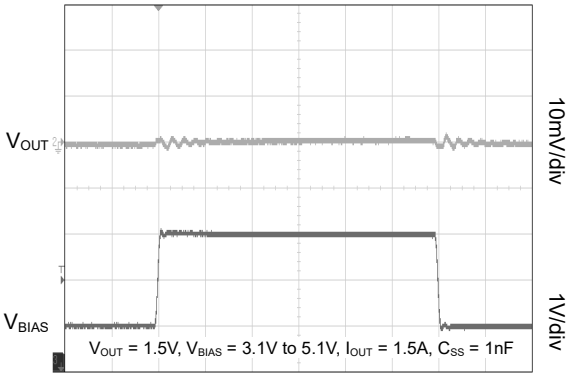
Time (10ms/div)

V_{IN} Line Transient Response



Time (50μs/div)

V_{BIAS} Line Transient Response

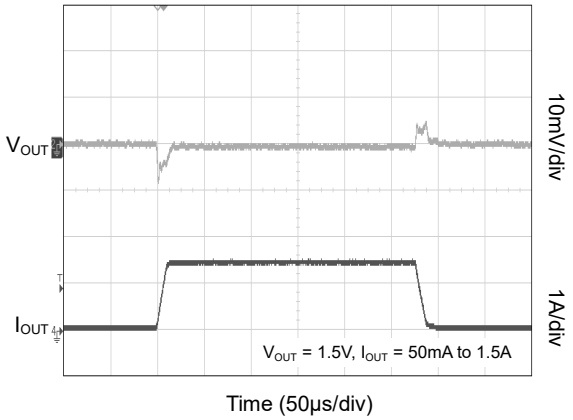


Time (50μs/div)

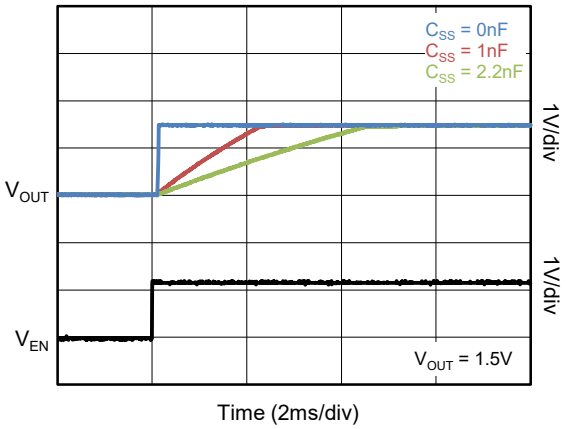
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 2.7V or (V_{OUT} + 1.6V), V_{EN} = V_{BIAS}, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 4.7μF, C_{OUT} = 10μF, unless otherwise noted.

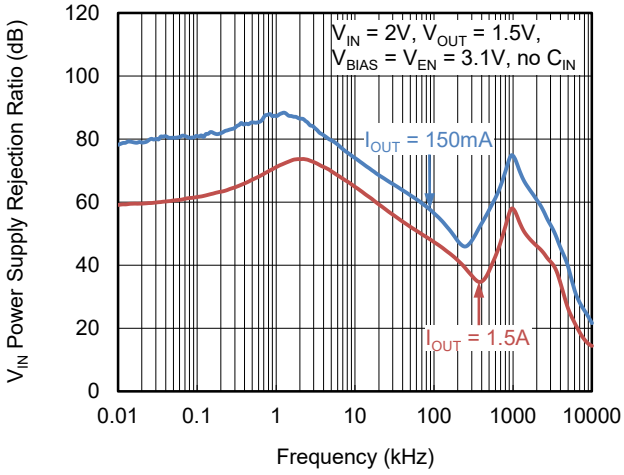
Load Transient Response



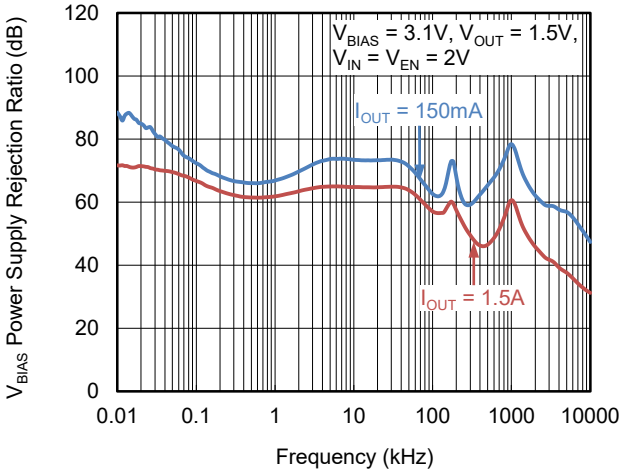
Turn-On Response



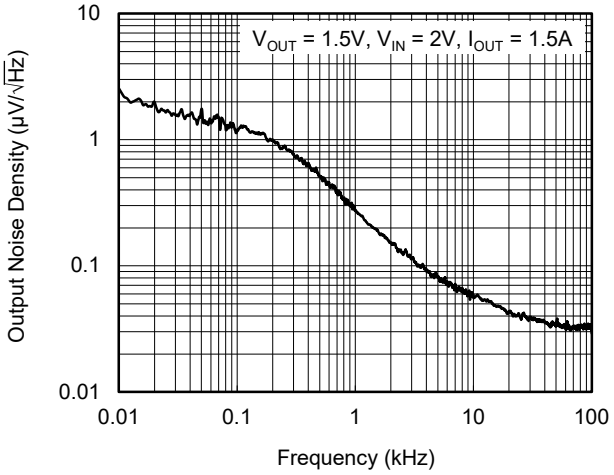
V_{IN} Power Supply Rejection Ratio vs. Frequency



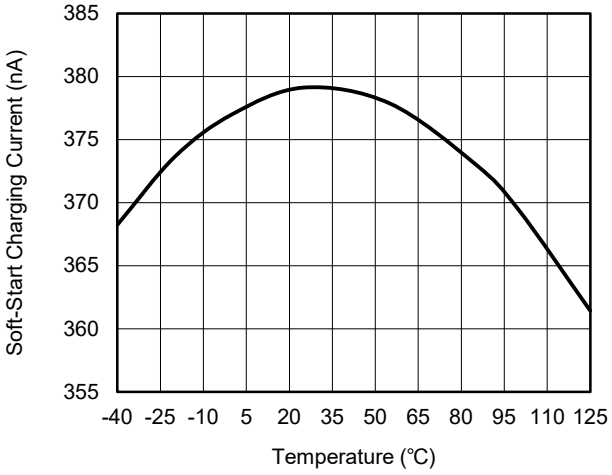
V_{BIAS} Power Supply Rejection Ratio vs. Frequency



Output Noise Density vs. Frequency



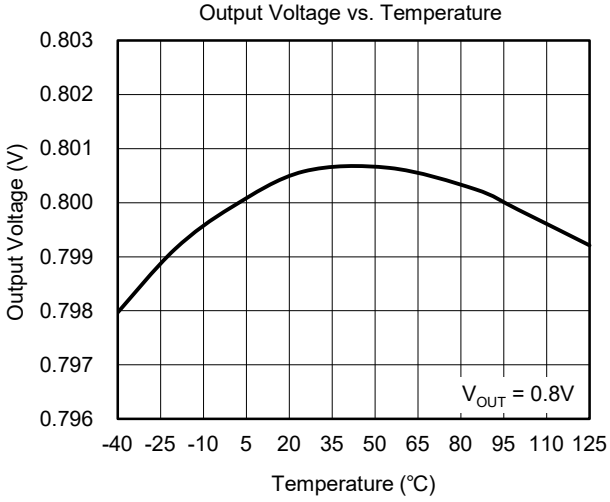
Soft-Start Charging Current vs. Temperature



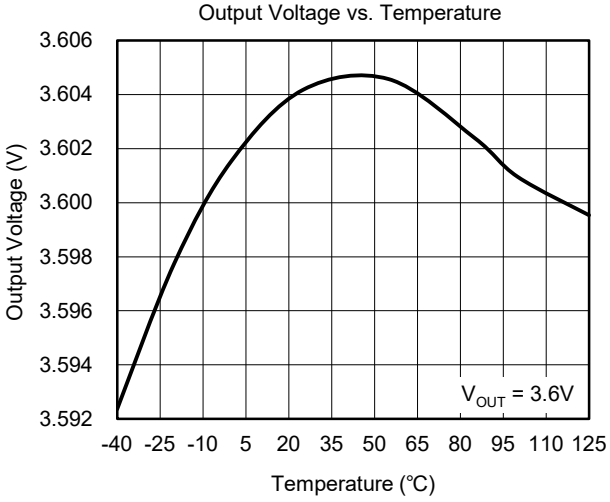
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 2.7V or (V_{OUT} + 1.6V), V_{EN} = V_{BIAS}, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 4.7μF, C_{OUT} = 10μF, unless otherwise noted.

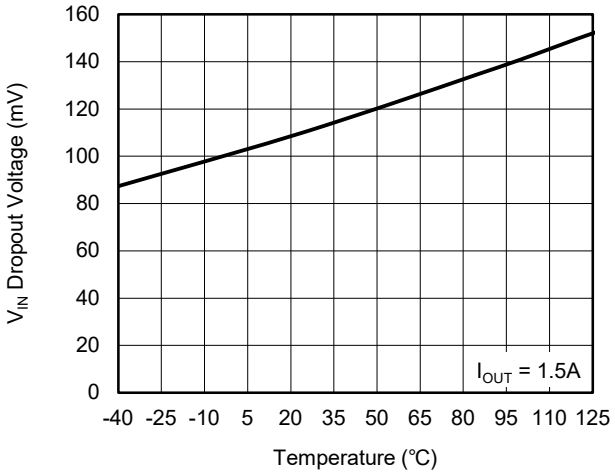
Output Voltage vs. Temperature



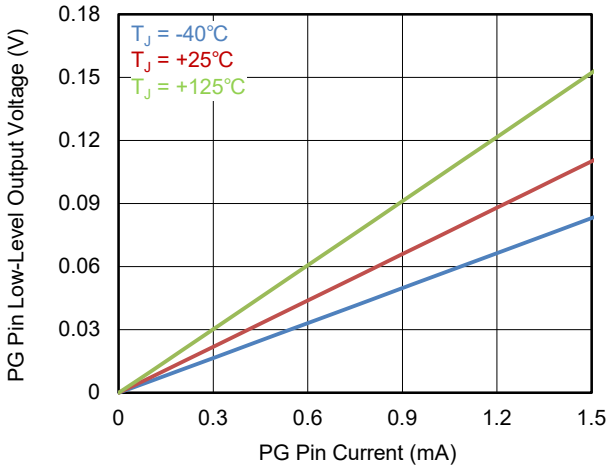
Output Voltage vs. Temperature



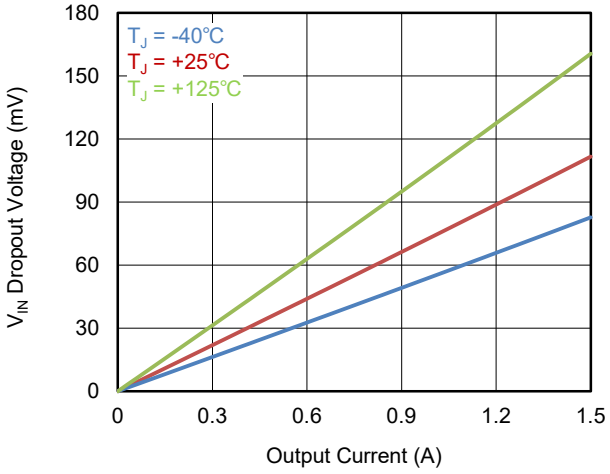
V_{IN} Dropout Voltage vs. Temperature



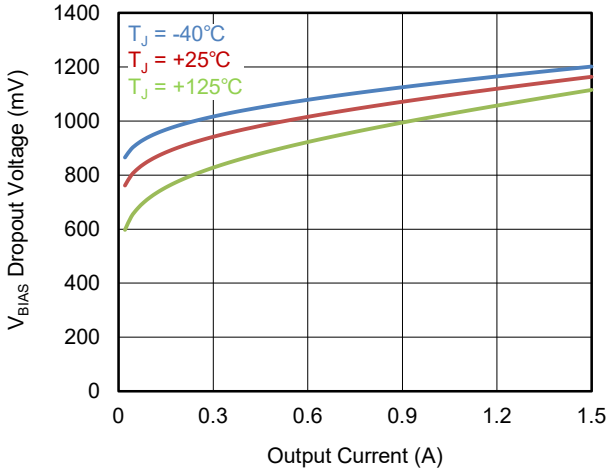
PG Pin Low-Level Output Voltage vs. PG Pin Current



V_{IN} Dropout Voltage vs. Output Current



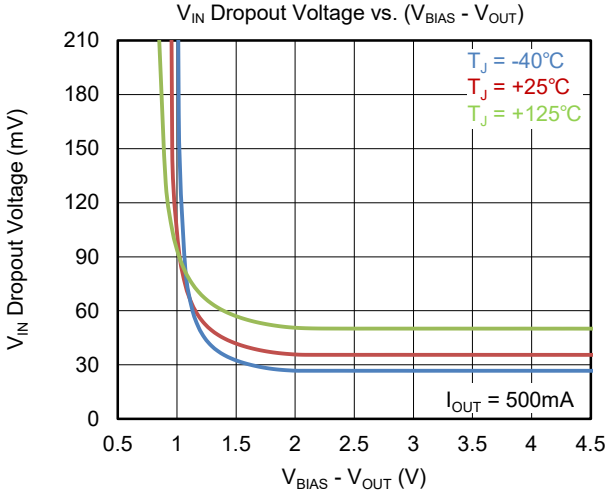
V_{BIAS} Dropout Voltage vs. Output Current



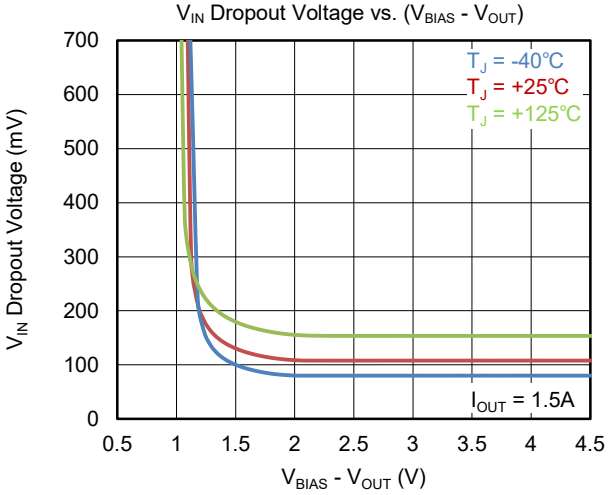
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 2.7V or (V_{OUT} + 1.6V), V_{EN} = V_{BIAS}, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 4.7μF, C_{OUT} = 10μF, unless otherwise noted.

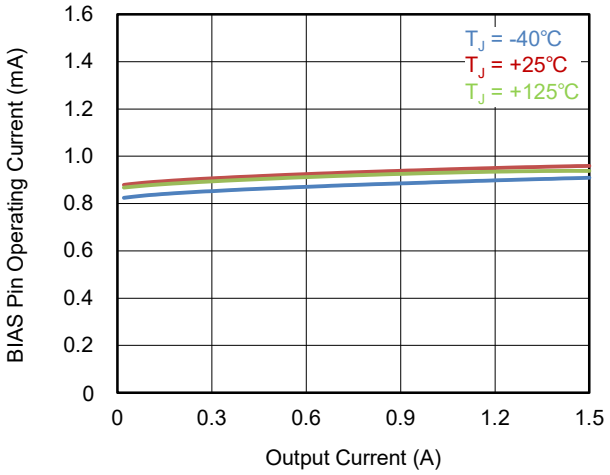
V_{IN} Dropout Voltage vs. (V_{BIAS} - V_{OUT})



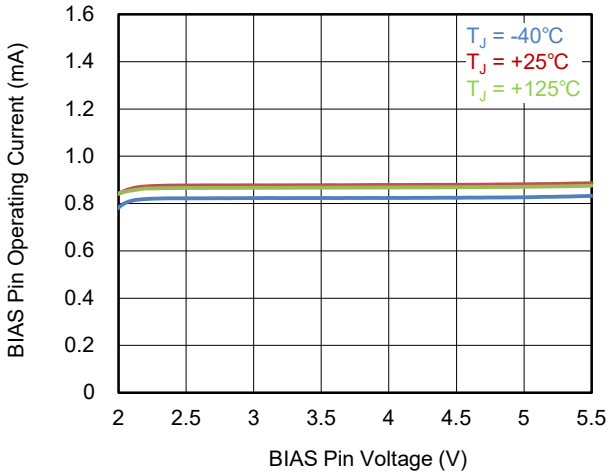
V_{IN} Dropout Voltage vs. (V_{BIAS} - V_{OUT})



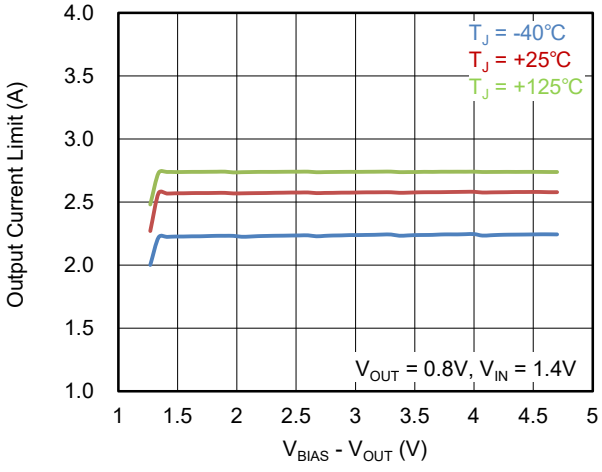
BIAS Pin Operating Current vs. Output Current



BIAS Pin Operating Current vs. BIAS Pin Voltage



Output Current Limit vs. (V_{BIAS} - V_{OUT})



APPLICATION INFORMATION

The SGM2069 is a low noise and low dropout LDO and provides 1.5A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2069 useful in a variety of applications. The SGM2069 provides protection functions for output overload, output short-circuit condition and overheating.

The SGM2069 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown ground current consumes as low as 0.1μA (TYP).

Input Capacitors Selection (C_{IN} and C_{BIAS})

The input decoupling capacitors should be placed as close as possible to the IN pin and BIAS pin to ensure the device stability. C_{IN} = 2.2μF and C_{BIAS} = 0.22μF or larger X7R or X5R ceramic capacitors are selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings. For C_{OUT} with larger capacitance, it is recommended to choose the larger capacitance C_{IN}.

Output Capacitor Selection (C_{OUT})

The output capacitor should be placed as close as possible to the OUT pin. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of C_{OUT} that SGM2069 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Soft-Start Capacitor Selection (C_{SS})

The SGM2069 is designed for a monotonic soft-start time of output rising, it can be achieved via an external capacitor (C_{SS}) on the SS pin. Using an external C_{SS} is recommended for general application. It is not only for the in-rush current minimization but also helps reduce the noise component from internal reference.

Dropout Voltage

The SGM2069 specifies two dropout voltages because there are two power supplies V_{IN} and V_{BIAS} and one V_{OUT} regulator output. When the output voltage is lower than 1.6V, V_{BIAS} dropout voltage does is not applicable because the minimum bias operating voltage is 2.7V.

When V_{OUT} begins to decrease and V_{BIAS} is high enough, the V_{IN} dropout voltage equals to V_{IN} - V_{OUT}. V_{BIAS} dropout voltage refers to V_{BIAS} - V_{OUT} when the IN and BIAS pins are connected together and V_{OUT} begins to decrease.

Adjustable Regulator

The output voltage of the SGM2069 can be adjusted from 0.8V to 3.6V. The FB pin will be connected to two external resistors as shown in Figure 3. The output voltage is determined by the following equation:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

V_{OUT} is output voltage and V_{ADJ} is the internal voltage reference, V_{ADJ} = 0.8V. Choose R_2 = 10kΩ to maintain an 80μA minimum load.

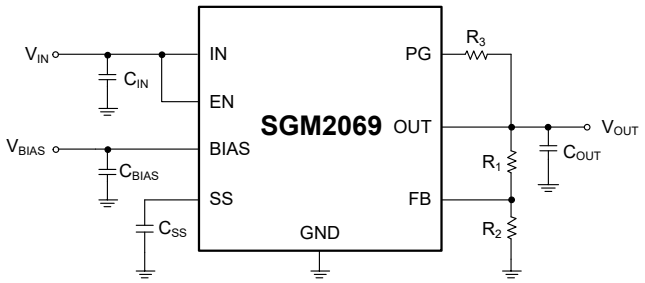


Figure 3. Adjustable Output Voltage Application

APPLICATION INFORMATION (continued)

Enable Operation

The SGM2069 uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.4V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 770Ω (TYP) resistor and the PG output is pulled down.

When the EN pin voltage is higher than 1.0V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{BIAS} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the IN pin and attempts to disable the output of the device if any of these rails collapses. The local input capacitance prevents severe brownouts in most applications. When the SGM2069 enters UVLO, the PG output is pulled down.

Power-Good Function

The SGM2069 features PG function for monitoring the feedback voltage, so as to reflect the state of the output voltage. When the output voltage is lower than PG_{LTH}, the PG pin open-drain engages and pulls the PG pin close to GND. When the output voltage is higher than PG_{HTH}, the PG pin is indicated as high impedance. Connecting the PG pin to an external power supply via a pull-up resistor enables any downstream device to receive a power-good valid logic signal for sequencing. The resistance range of the pull-up resistor is recommended to be between 10kΩ and 100kΩ.

The PG output is pulled down when the SGM2069 is in one of the following states, including disabled, thermal shutdown, or UVLO.

Reverse Current Protection

The pass transistor has an inherent body diode which will be forward biased in the case when V_{OUT} > (V_{IN} + 0.3V). If extended reverse voltage operation is anticipated, external limiting might be appropriate.

Negatively Biased Output

When the output voltage is negative, the chip may not start up due to parasitic effects. Ensure that the output is greater than -0.3V under all conditions. If negatively biased output is excessive and expected in the application, a Schottky diode can be added between the OUT pin and GND pin.

Output Current Limit and Short-Circuit Protection

When overload events happen, the output current is internally limited to 2.6A (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 0.95A (TYP).

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2069 will be in shutdown state and it will remain in this state until the die temperature decreases to +140℃. When the device enters thermal shutdown, the PG output is pulled low.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2069 can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2069 is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (2)$$

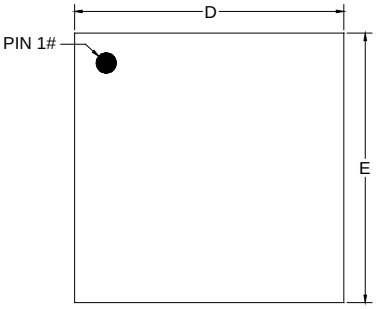
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

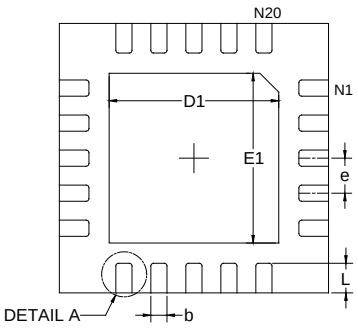
Changes from Original (MAY 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

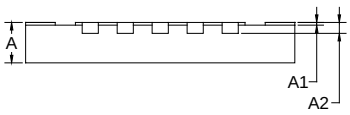
TQFN-5×5-20L



TOP VIEW

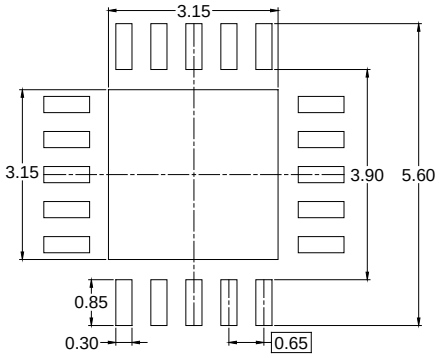


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



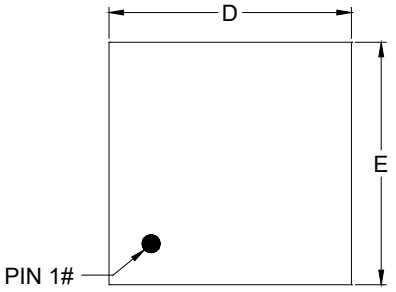
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	4.950	5.000	5.050
D1	3.100	3.150	3.200
E	4.950	5.000	5.050
E1	3.100	3.150	3.200
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.500	0.550	0.600

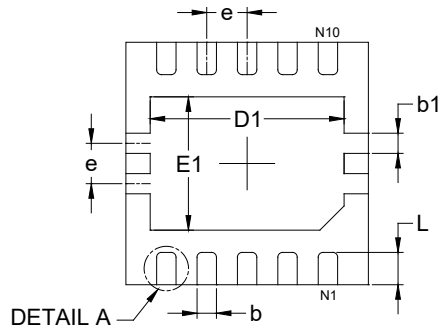
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

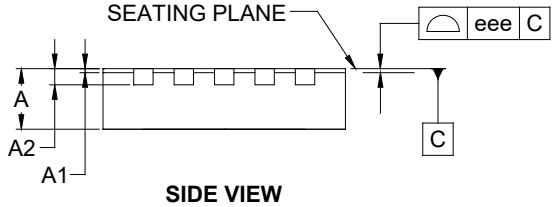
TDFN-3×3-10AL



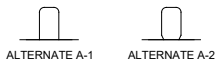
TOP VIEW



BOTTOM VIEW

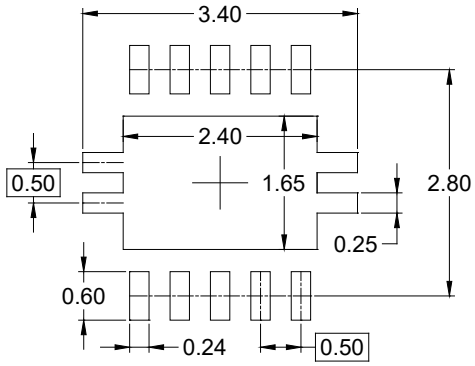


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



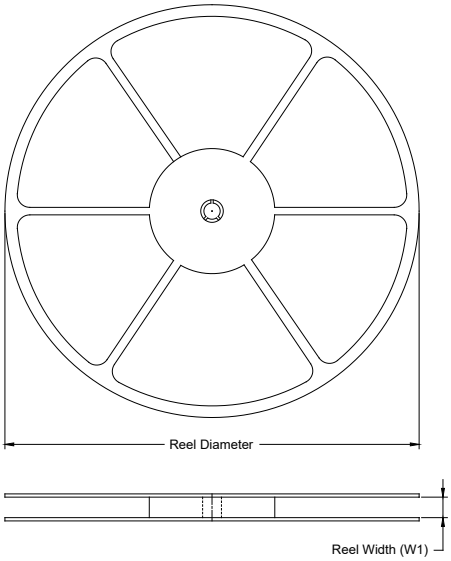
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
b1	0.250 REF		
D	2.900	-	3.100
E	2.900	-	3.100
D1	2.300	-	2.500
E1	1.550	-	1.750
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

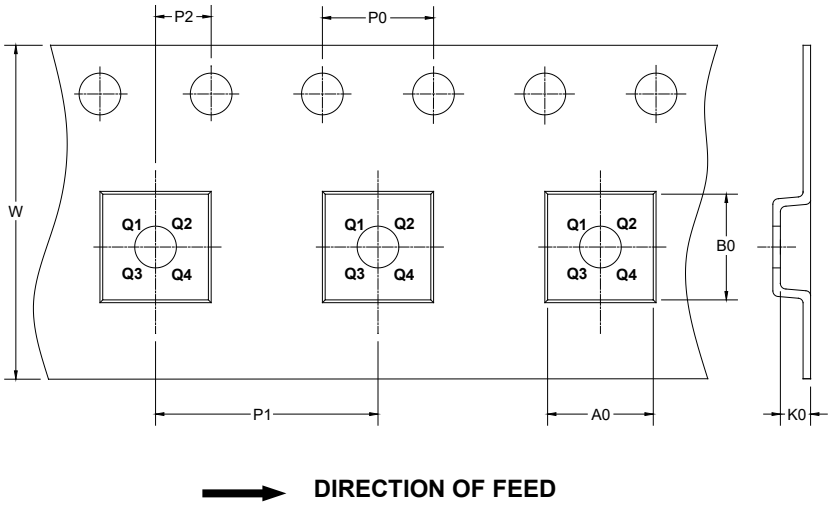
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



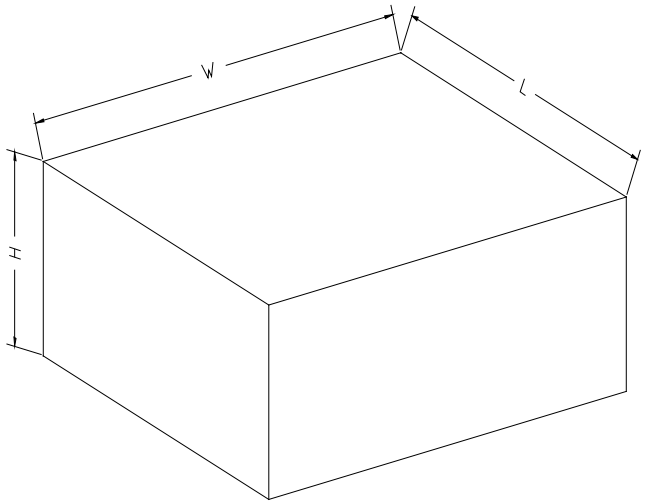
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-20L	13"	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2
TDFN-3×3-10AL	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002