SGM3852
PMIC for LTPO and Tandem AMOLED Display

GENERAL DESCRIPTION

The SGM3852 is designed for powering LTPO (Low Temperature Polycrystalline Oxide) and Tandem structure AMOLED displays which require V_{ELVDD}, V_{ELVSS}, V_{AVDD}, V_{DVDD} and V_{VGL}.

The device integrates two Buck converters VO1 for V_{ELVDD} and VO4 for V_{DVDD}, one Boost converter VO3 for V_{AVDD}, one dual-phase inverting Buck-Boost converter VO2 for V_{ELVSS} and one single-phase inverting Buck-Boost converter VO5 for V_{VGL}. Output voltages of all the five converters can be programmed in digital steps through the I^2C interface.

The SGM3852 is available in a Green WLCSP-3.2×2.8-56B package.

FEATURES

- **3.0V to 5.0V Input Supply Voltage Range**
- **Synchronous Buck Converter VO1 (ELVDD)**
  - **2.0V to 3.0V Output Voltage with 100mV Steps**
  - **2.8V Default Output Voltage**
  - **1% Accuracy at 2.8V**
  - **1.4A Output Current Capability**
- **Synchronous Inverting Buck-Boost Converter VO2 (ELVSS)**
  - **-2V to -12V Output Voltage with 50mV Steps**
  - **-4.8V Default Output Voltage**
  - **0.4% Initial Accuracy at -4.8V**
  - **1.45A Output Current Capability @-4V**
  - **1A Output Current Capability @-6.8V**
  - **730mA Output Current Capability @ -10V**
  - **590mA Output Current Capability @-12V**
- **Synchronous Boost Converter VO3 (AVDD)**
  - **5.5V to 7.9V Output Voltage with 100mV Steps**
  - **6.5V Default Output Voltage**
  - **1% Accuracy at 6.5V**
  - **250mA Output Current Capability**
- **Synchronous Buck Converter VO4 (DVDD)**
  - **0.8V to 1.5V Output Voltage with 10mV Steps**
  - **1.0V/1.2V/1.3V Default Output Voltage Options**
  - **0.5% Initial Accuracy at 1.2V**
  - **400mA Output Current Capability**
- **Synchronous Inverting Buck-Boost Converter VO5 (VGL)**
  - **-5V to -15V Output Voltage with 100mV Steps**
  - **-11V Default Output Voltage**
  - **1% Accuracy at -11V**
  - **40mA Output Current Capability**
- **V_{IN} and V_{OUT} Bi-Directional Isolation for ELVSS/AVDD/VGL**
  - **Each V_{IN} Supports Discrete Power Supply**
- **I^2C Interface**
- **Under-Voltage Lockout (UVLO)**
- **All Channels Soft-Start**
- **All Channels Fast Discharge Function (FD)**
- **All Channels Short Circuit Protection (SCP)**
- **All Channels Over-Circuit Protection (OCP)**
- **Over-Temperature Protection (OTP)**
- **Overload Protection (OLP)**
- **Start-Up Short Detection (SSD)**
- **V_{ELVSS} Start-Up Delay: 5.7ms**
- **Short Circuit and OLP Detection Time: 1ms**
- **Available in a Green WLCSP-3.2×2.8-56B Package**

APPLICATIONS

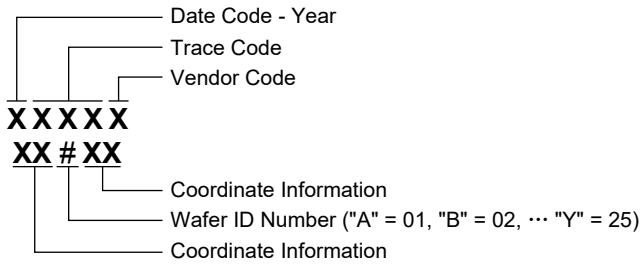
Smartphones & Tablets
Folding-Screen Phones
LTPO2.0 AMOLED Displays
Tandem AMOLED Displays

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3852	WLCSP-3.2×2.8-56B	-40℃ to +85℃	SGM3852YG/TR	0GI XXXXX XX#XX	Tape and Reel,1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to Ground Pin)
PVIN1, PVIN2A, PVIN2B Voltages ..... -0.3V to 6V
PVIN4, PVIN5, AVIN Voltages ..... -0.3V to 6V
DVDD_EN, DVDD_SEL Voltages ..... -0.3V to 6V
SCL, SDA, nINT, nRESET Voltages ..... -0.3V to 6V
ELVDD_FB, DVDD_FB Voltages ..... -0.3V to 6V
ELVSSA, ELVSSB, ELVSS_FB Voltages ..... -13V to 0.3V
VGL Voltage ..... -16V to 0.3V
SW1, SW4 Voltages ..... -0.3V to 6V
SW1, SW4 Voltages (Transient: 10ns) ..... -1V to 8V
SW1, SW4 Voltages (Transient: 60ns) ..... -0.75V to 8V
SW1, SW4 Voltages (Transient: 100ns) ..... -0.5V to 8V
SW3, AVDD Voltages ..... -0.3V to 10V
SW3 Voltage (Transient: 10ns) ..... -1V to 12V
SW3 Voltages (Transient: 60ns) ..... -0.75V to 12V
SW3 Voltages (Transient: 100ns) ..... -0.5V to 12V
SW2A, SW2B Voltages ..... -13V to 6V
SW2A, SW2B Voltages (Transient: 10ns) ..... -15V to 8V
SW5 Voltage ..... -16V to 6V
SW5 Voltage (Transient: 10ns) ..... -18V to 8V
PVIN5 - SW5 Voltage ..... -0.3V to 21V
Package Thermal Resistance
WLCSP-3.2×2.8-56B, θ_{JA} ..... 30℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

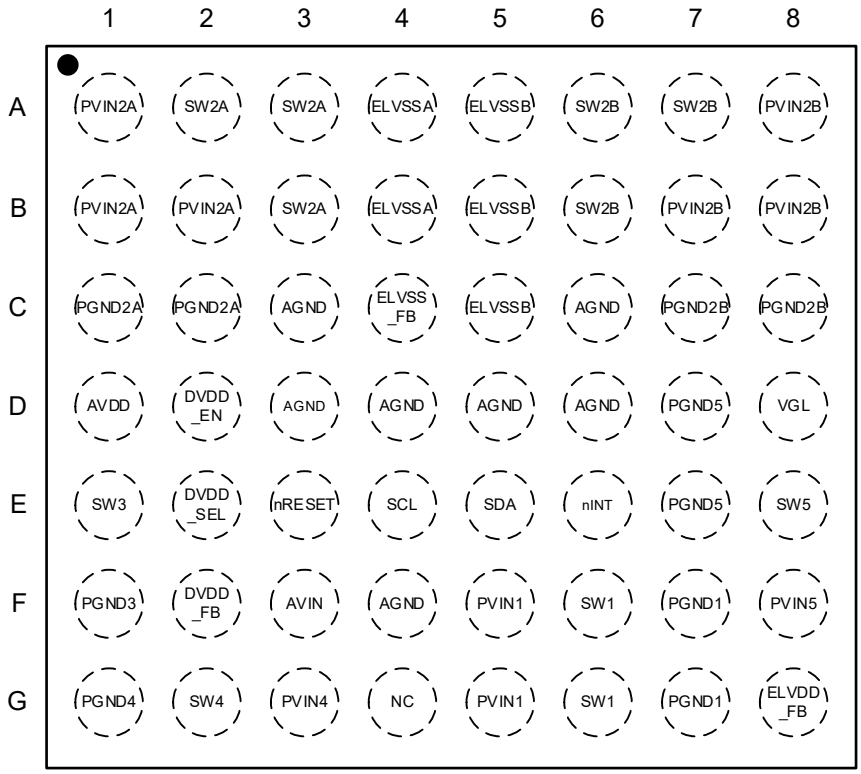
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.2×2.8-56B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1, B1, B2	PVIN2A	P	ELVSS Inverting Buck-Boost Converter Phase A Power Supply Input Pin.
A2, A3, B3	SW2A	P	ELVSS Inverting Buck-Boost Converter Phase A Switching Node.
A4, B4	ELVSSA	P	ELVSS Inverting Buck-Boost Converter Phase A Output Pin.
A5, B5, C5	ELVSSB	P	ELVSS Inverting Buck-Boost Converter Phase B Output Pin.
A6, A7, B6	SW2B	P	ELVSS Inverting Buck-Boost Converter Phase B Switching Node.
A8, B7, B8	PVIN2B	P	ELVSS Inverting Buck-Boost Converter Phase B Power Supply Input Pin.
C1, C2	PGND2A	G	ELVSS Inverting Buck-Boost Converter Phase A Power Ground Pin.
C3, C6, D3, D4, D5, D6, F4	AGND	G	Analog Ground Pin.
C4	ELVSS_FB	I	ELVSS Inverting Buck-Boost Converter Output Sense Input.
C7, C8	PGND2B	G	ELVSS Inverting Buck-Boost Converter Phase B Power Ground Pin.
D1	AVDD	P	AVDD Boost Converter Output Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	DESCRIPTION
D2	DVDD_EN	I	DVDD Buck Converter Enable Pin.
D7, E7	PGND5	G	VGL Inverting Buck-Boost Converter Power Ground Pin.
D8	VGL	P	VGL Inverting Buck-Boost Converter Output Pin.
E1	SW3	P	AVDD Boost Converter Switching Node.
E2	DVDD_SEL	I	DVDD Default Output Voltage Selection Pin. High = 1.0V; Low = 1.2V; Floating = 1.3V.
E3	nRESET	I	Reset Control Pin.
E4	SCL	I	Clock Input Pin for the I^2C Serial Interface.
E5	SDA	I/O	Data I/O Pin for the I^2C Serial Interface.
E6	nINT	O	Open-Drain Interrupt Output.
E8	SW5	P	VGL Buck-Boost Converter Switching Node.
F1	PGND3	G	AVDD Boost Converter Power Ground Pin.
F2	DVDD_FB	I	DVDD Buck Converter Output Sense Input.
F3	AVIN	P	Analog Power Supply.
F5, G5	PVIN1	P	ELVDD Buck Converter Power Supply Input Pin.
F6, G6	SW1	P	ELVDD Buck Converter Switching Node.
F7, G7	PGND1	G	ELVDD Buck Converter Power Ground Pin.
F8	PVIN5	P	VGL Inverting Buck-Boost Converter Power Supply Input Pin.
G1	PGND4	G	DVDD Buck Converter Power Ground Pin.
G2	SW4	P	DVDD Buck Converter Switching Node.
G3	PVIN4	P	DVDD Buck Converter Power Supply Input Pin.
G4	NC	I	No Connection.
G8	ELVDD_FB	I	ELVDD Buck Converter Output Sense pin.

NOTE: I: input, O: output, I/O: input and output, P: power, G: ground.

TYPICAL APPLICATION

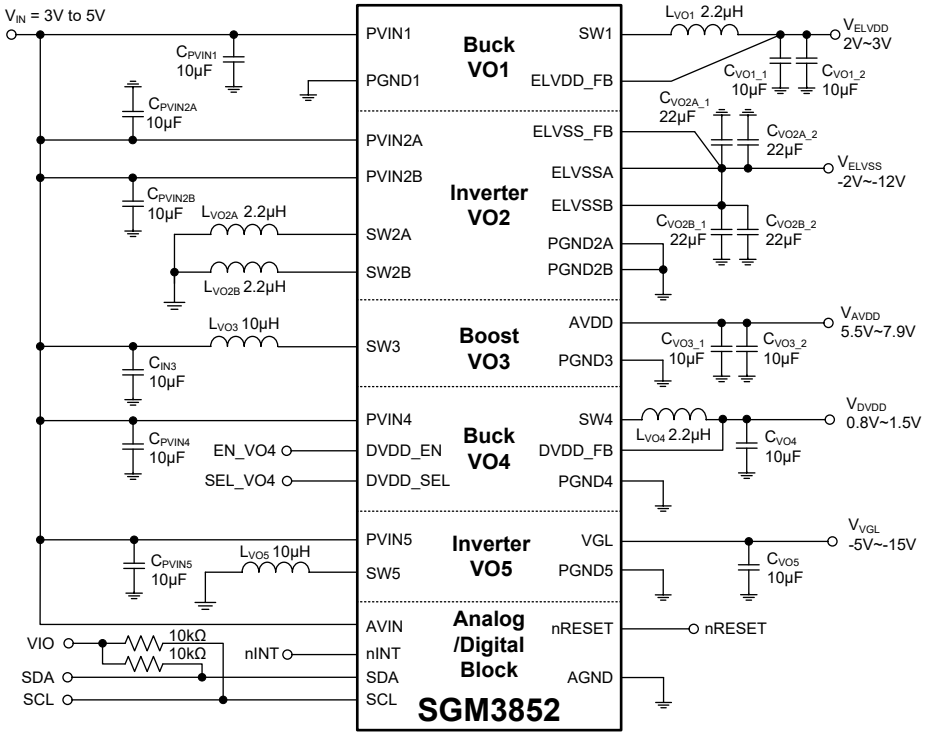


Figure 1. Typical Application Circuit

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended Component Selection

Converter	Component	Value	Number	Electrical Spec	Part Number	Manufacturer
ELVDD	C_{PVIN1}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO1_1} C_{VO1_2}	10μF	2	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	L_{VO1}	2.2μH	1	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
		4.7μH	1	1.9A, 100mΩ, 252010	HTEH25201T-4R7MSR	Cyntec
ELVSS	C_{PVIN2A} C_{PVIN2B}	10μF	2	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO2A_1}, C_{VO2A_2} C_{VO2B_1}, C_{VO2B_2}	22μF	4	X5R, 25V, 0805	GRM21BR61E226ME44#	Murata
	L_{VO2A} L_{VO2B}	2.2μH	2	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
AVDD	C_{IN3}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO3_1} (1) C_{VO3_2} (1)	10μF	2	X5R, 16V, 0603	GRM188R61C106KAAL	Murata
	L_{VO3}	10μH	1	1.3A, 390mΩ, 252012	SDEM25201B-100MS	Cyntec
DVDD	C_{PVIN4}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO4}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	L_{VO4}	2.2μH	1	2.7A, 98mΩ, 252012	SDEM25201B-1R2MS	Cyntec
VGL	C_{PVIN5}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO5}	10μF	1	X5R, 25V, 0805	GRM219R61C226ME15	Murata
	L_{VO5}	10μH	1	1.3A, 390mΩ, 252012	SDEM25201B-100MS	Cyntec

NOTE: 1. C_{VO3_1} = C_{VO3_2} = 10μF×2 are recommended when I_{VO3} > 150mA.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.7V, V_{ELVDD} = 2.8V, V_{ELVSS} = -4.8V, V_{AVDD} = 6.5V, V_{DVDD} = 1.2V, V_{VGL} = -11V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current and Thermal Protection							
Input Voltage Range	V_{IN}			3		5	V
Shutdown Current into PVINx, AVIN	I_{SD}	All channels off			0.8	2.0	μA
Quiescent Current into PVINx, AVIN	I_{QON}	All channels on, no load	L_{VO1} = 2.2μH		3.60		mA
			L_{VO1} = 4.7μH		3		
Under-Voltage Lockout Threshold (AVIN)	V_{IT-}	V_{IN} falling		2.10	2.25	2.40	V
	V_{IT+}	V_{IN} rising		2.20	2.36	2.50	
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising			150		℃
		Junction temperature falling			135		
Buck Converter (V_{VO1} = V_{ELVDD})							
Positive Output 1 Voltage	V_{VO1}	2V to 3V with 0.1V/step, default 2.8V		2	2.8	3	V
Positive Output 1 Voltage Accuracy		V_{VO1} = 2.8V, no load	T_J = +25℃	-0.8		0.8	%
			T_J = -40℃ to +85℃	-1		1	
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 200mA			105		mΩ
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 200mA			100		
SW1 Switch Current Limit	I_{SW1}	T_J = +25℃		1.9	2.3	2.8	A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA		1.3	1.45	1.6	MHz
Output Current Capability	I_{VO1}	V_{IN} = 3.3V to 5V, T_J = +25℃		1400			mA
Short Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal V_{VO1}, T_J = +25℃		68	82	90	%
VO1 Discharge Resistance	$R_{VO1(DCG)}$	I_{VO1} = 20mA			75		Ω
VO1 Discharge Time	t_{DVO1}				2.2		ms
Efficiency	$Eff_{VO1-VO2}$	V_{IN} = 3.7V, V_{VO1} = 2.8V, V_{VO2} = -4.8V, I_{VO1_VO2} = 40mA to 70mA			89.6		%
		V_{IN} = 3.7V, V_{VO1} = 2.8V, V_{VO2} = -7.4V, I_{VO1_VO2} = 100mA			88.8		
		V_{IN} = 3.7V, V_{VO1} = 2.8V, V_{VO2} = -9.0V, I_{VO1_VO2} = 450mA			87.8		
Line Transient	$VO1_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 0mA to 300mA	Overshoot		8		mV
			Undershoot		8		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 300mA to 1400mA	Overshoot		8		mV
			Undershoot		8		
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 3V to 5V			±0.010		%/V
		No load, V_{IN} = 3V to 5V			±0.007		
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1} = 0mA to 700mA			5		mV_{PP}
		I_{VO1} = 700mA to 1400mA			6		mV_{PP}
Load Transient	$VO1_{LOADTRA}$	ΔI_{VO1} = 10mA to 1400mA, t_R = t_F = 5ms	Overshoot		3		mV
			Undershoot		3		
Load Regulation	$VO1_{LOADREG}$	0mA ≤ I_{VO1} ≤ 1400mA, V_{IN} = 3.3V to 5V			3		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{ELVDD} = 2.8V, V_{ELVSS} = -4.8V, V_{AVDD} = 6.5V, V_{DVDD} = 1.2V, V_{VGL} = -11V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Buck-Boost Converter (V_{VO2} = V_{ELVSS})							
Negative Output Voltage Range	V_{VO2}	-12V to -2V with 50mV/step, default -4.8V		-12	-4.8	-2	V
Negative Output Voltage Accuracy (Initialization)		V_{VO2} = -4.8V, no load, T_J = +25℃		-20		20	mV
		V_{VO2} = -9V, no load, T_J = +25℃		-0.6		0.6	%
		V_{VO2} = -12V, no load, T_J = +25℃		-0.9		0.9	%
SW2 MOSFET On-Resistance-Phase A	$R_{DS(ON)A1}$	I_{DS} = 200mA			95		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase A	$R_{DS(ON)A2}$	I_{DS} = 200mA			55		
SW2 MOSFET On-Resistance-Phase B	$R_{DS(ON)B1}$	I_{DS} = 200mA			95		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase B	$R_{DS(ON)B2}$	I_{DS} = 200mA			55		
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA		1.1	1.25	1.4	MHz
Output Current Capability	I_{VO2}	V_{IN} = 3V to 5V, V_{VO2} = -4V, T_J = +25℃		1450			mA
		V_{IN} = 3V to 5V, V_{VO2} = -6.8V, T_J = +25℃		1000			
		V_{IN} = 3V to 5V, V_{VO2} = -10V, T_J = +25℃		730			
		V_{IN} = 3V to 5V, V_{VO2} = -12V, T_J = +25℃		590			
SW2 Switch Current Limit-Phase A	I_{SW2A}	Inductor peak current, T_J = +25℃		2.8	3.5	4.2	A
SW2 Switch Current Limit-Phase B	I_{SW2B}	Inductor peak current, T_J = +25℃		2.8	3.5	4.2	A
Average Load Current Threshold with Dual-Phase	$I_{RMSA\&B}$	Load current rising			340		mA
Average Load Current Threshold with Phase A Only	I_{RMSA}	Load current falling			240		mA
Short Circuit Threshold during start-up after 20ms	$V_{VO2(SCP)}$	Percentage of nominal V_{VO2}, T_J = +25℃		82	87	91	%
VO2 Discharge Resistance	$R_{VO2(DCG)}$	I_{VO2} = 20mA			25		Ω
VO2 Discharge Time	t_{DVO2}				1.30		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}				1.0	2.2	μA
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO2} = 0mA to 750mA, V_{VO2} = -2V to -6V			11		mV_{PP}
		I_{VO2} = 0mA to 1400mA, V_{VO2} = -2V to -6V			12		mV_{PP}
		I_{VO2} = 0mA to 400mA, V_{VO2} = -9V to -12V			17		mV_{PP}
		I_{VO2} = 0mA to 700mA, V_{VO2} = -9V to -12V			18		mV_{PP}
Line Transient	$VO2_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 0mA to 750mA, V_{VO2} = -2V to -6V	Overshoot		16		mV
			Undershoot		18		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 750mA to 1400mA, V_{VO2} = -2V to -6V	Overshoot		23		mV
			Undershoot		33		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 0mA to 400mA, V_{VO2} = -9V to -12V	Overshoot		16		mV
			Undershoot		19		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 400mA to 700mA, V_{VO2} = -9V to -12V	Overshoot		24		mV
			Undershoot		30		
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 3V to 5V			±0.007		%/V
Load Transient	$VO2_{LOADTRA}$	ΔI_{VO2} = 10mA to 1400mA, V_{VO2} = -4.8V, t_R = t_F = 5ms	Overshoot		28		mV
			Undershoot		17		
Load Regulation	$VO2_{LOADREG}$	0mA ≤ I_{VO2} ≤ 1400mA			±0.024		%/A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{ELVDD} = 2.8V, V_{ELVSS} = -4.8V, V_{AVDD} = 6.5V, V_{DVDD} = 1.2V, V_{VGL} = -11V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Converter (V_{VO3} = V_{AVDD})							
Positive Output 3 Voltage Range	V_{VO3}	5.5V to 7.9V with 0.1V/step, default 6.5V		5.5	6.5	7.9	V
Positive Output 3 Voltage Accuracy		V_{VO3} = 6.5V, no load	T_J = +25℃	-0.8		0.8	%
			T_J = -40℃ to +85℃	-1		1	
SW3 MOSFET On-Resistance	$R_{DS(ON)31}$	I_{DS} = 200mA			220		mΩ
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)32}$	I_{DS} = 200mA			560		
SW3 Switch Current Limit	I_{SW3}	Inductor peak current, T_J = +25℃		0.9	1.35	1.75	A
SW3 Switching Frequency	f_{SW3}	I_{VO3} = 30mA		1.3	1.45	1.6	MHz
Output Current Capacity	I_{VO3}	V_{IN} = 3V to 5V, T_J = +25℃		250			mA
Short Circuit Threshold in Operation	$V_{VO3(SCP)}$	Percentage of nominal V_{VO3}, T_J = +25℃		84	89	93	%
VO3 Leakage, No Discharge	I_{LEAK_VO3}				1.2	2.1	μA
VO3 Discharge Resistance	$R_{VO3(DCG)}$	I_{VO3} = 20mA			50		Ω
VO3 Discharge Time	t_{DVO3}				1.7		ms
Efficiency	Eff_{VO3}	V_{IN} = 3.7V, I_{VO3} = 5mA to 25mA			93.2		%
		V_{IN} = 3.7V, I_{VO3} = 25mA to 100mA			94.8		%
Output Voltage Ripple	$VO3_{RIPPLE}$	I_{VO3} = 0mA to 250mA			17		mV_{PP}
Line Transient	$VO3_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO3} = 30mA	Overshoot		10		mV
			Undershoot		9		
Line Regulation	$VO3_{LINEREG}$	I_{VO3} = 100mA, V_{IN} = 3V to 5V			±0.009		%/V
Load Transient	$VO3_{LOADTRA}$	ΔI_{VO3} = 10mA to 60mA, t_R = t_F = 10μs, V_{IN} = 3.8V	Overshoot		44		mV
			Undershoot		51		
		ΔI_{VO3} = 200mA to 250mA, t_R = t_F = 10μs, V_{IN} = 3.8V	Overshoot		44		mV
			Undershoot		43		
Load Regulation	$VO3_{LOADREG}$	0mA ≤ I_{VO3} ≤ 250mA			±0.09		%/A
Buck Converter (V_{VO4} = V_{DVDD})							
Positive Output 4 Voltage Range	V_{VO4}	0.8V to 1.5V with 10mV/step, default 1.3V/1.2V/1.0V		0.8	1.3 1.2 1.0	1.5	V
Positive Output 4 Voltage Accuracy (Initialization)		V_{VO4} = 1.2V, T_J = +25℃		-6		6	mV
Positive Output 4 Voltage Accuracy		V_{VO4} = 1.2V	T_J = +25℃	-12		12	mV
			T_J = -40℃ to +85℃	-26		26	mV
SW4 MOSFET On-Resistance	$R_{DS(ON)41}$	I_{DS} = 200mA			350		mΩ
SW4 MOSFET Rectifier On-Resistance	$R_{DS(ON)42}$	I_{DS} = 200mA			220		
SW4 Switch Current Limit	I_{SW4}	Inductor peak current, T_J = +25℃		0.75	1.00	1.3	A
SW4 Switching Frequency	f_{SW4}	I_{VO4} = 400mA			1.75		MHz
Output Current Capacity	I_{VO4}	V_{IN} = 3V to 5V, T_J = +25℃		400			mA
VO4 Discharge Resistance	$R_{VO4(DCG)}$	I_{VO4} = 20mA			75		Ω
VO4 Discharge Time	t_{DVO4}				1.4		ms
Short Circuit Threshold in Operation	$V_{VO4(SCP)}$	Percentage of nominal V_{VO4}, T_J = +25℃		82	87	93	%
Efficiency	Eff_{VO4}	V_{IN} = 3.7V, V_{VO4} = 1.2V, I_{VO4} = 60mA to 100mA			87.6		%
Output Voltage Ripple	$VO4_{RIPPLE}$	I_{VO4} = 0mA to 400mA			19		mV_{PP}

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{ELVDD} = 2.8V, V_{ELVSS} = -4.8V, V_{AVDD} = 6.5V, V_{DVDD} = 1.2V, V_{VGL} = -11V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Transient	$VO4_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO4} = 200mA	Overshoot		10		mV
			Undershoot		10		
Line Regulation	$VO4_{LINEREG}$	I_{VO4} = 60mA to 100mA, V_{IN} = 3V to 5V			±0.015		%/V
Load Transient	$VO4_{LOADTRA}$	ΔI_{VO4} = 100mA, t_R = t_F = 10μs, V_{IN} = 3V to 5V	Overshoot		27		mV
			Undershoot		16		
Load Regulation	$VO4_{LOADREG}$	0mA ≤ I_{VO4} ≤ 400mA			1		mV
Buck-Boost Converter (V_{VO5} = V_{VGL})							
Negative Output Voltage Range	V_{VO5}	-15V to -5V with 100mV/step, default -11V		-15	-11	-5	V
Negative Output Voltage Accuracy		V_{VO5} = -11V, no load	T_J = +25℃	-0.8		0.8	%
			T_J = -40℃ to +85℃	-1		1	
SW5 Switch Current Limit	I_{SW5_LIM}	Inductor peak current, T_J = +25℃		0.75	1.00	1.35	A
SW5 MOSFET On-Resistance	$R_{DS(ON)51}$	I_{DS} = 200mA			730		mΩ
SW5 MOSFET Rectifier On-Resistance	$R_{DS(ON)52}$	I_{DS} = 200mA			350		
SW5 Switching Frequency	f_{SW5}	I_{VO5} = 30mA		1.1	1.25	1.4	MHz
Output Current Capability	I_{VO5}	V_{IN} = 3V to 5V, T_J = +25℃		40			mA
Short Circuit Threshold during Start-Up after 20ms	$V_{VO5(SCP)}$	Percentage of nominal V_{VO5}, T_J = +25℃		71	82	91	%
VO5 Discharge Resistance	$R_{VO5(DCG)}$	I_{VO5} = 20mA			120		Ω
VO5 Discharge Time	t_{DVO5}				1.6		ms
VO5 Leakage, No Discharge	I_{LEAK_VO5}				1.1	2.2	μA
Output Voltage Ripple	$VO5_{RIPPLE}$	I_{VO5} = 0mA to 40mA			32		mV_{PP}
Line Transient	$VO5_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO5} = 0mA to 40mA	Overshoot		30		mV
			Undershoot		28		
Line Regulation	$VO5_{LINEREG}$	I_{VO5} = 5mA, V_{IN} = 3V to 5V			±0.006		%/V
Load Transient	$VO5_{LOADTRA}$	ΔI_{VO5} = 0mA to 10mA, V_{VO5} = -11V, t_R = t_F = 10μs	Overshoot		19		mV
			Undershoot		21		
Load Regulation	$VO5_{LOADREG}$	0mA ≤ I_{VO5} ≤ 40mA			±0.031		%/A
Logic Signals (DVDD_EN, nRESET)							
Logic Input High Level Voltage	V_{IH}			1			V
Logic Input Low Level Voltage	V_{IL}					0.4	V
Pull-Down Resistor	R_{DOWN}				520		kΩ
Open Drain Logic Signals (nINT)							
Logic Output High Level Voltage	V_H	I_{OH} = 0mA, V_{PULL_UP} = 1.8V, R_{PULL_UP} = 10kΩ		1.6		2.2	V
Logic Output Low Level Voltage	V_L	Sink 1mA				0.4	V
Logic Signals (SCL, SDA)							
Logic Input High Level Voltage	V_{IH}			1.0			V
Logic Input Low Level Voltage	V_{IL}					0.4	V
Logic Output High Level Voltage	V_{OH}			1.0			V
Logic Output Low Level Voltage	V_{OL}					0.4	V

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short Circuit Timer					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$	1.5	2.5	3.5	ms
VO1 Short Circuit Detection Time in Operation		0.8	1	1.3	
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$	5.8	6.7	7.9	
VO2 Short Circuit Detection Time in Operation		0.8	1	1.3	
VO3 Short Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$		3.0		
VO3 Short Circuit Detection Time in Operation		0.8	1	1.3	
VO4 Short Circuit Detection Time in Start-Up	$t_{VO4(SCP)}$		3.6		
VO4 Short Circuit Detection Time in Operation		0.8	1	1.3	
VO5 Short Circuit Detection Time in Start-Up	$t_{VO5(SCP)}$		2.2		
VO5 Short Circuit Detection Time in Operation		0.8	1	1.3	
Power Sequence					
VO1 Start-Up Time	t_{SS1}		1.5		ms
VO2 Start-Up Time	t_{SS2}		2.3		
VO2 Start-Up Time Delay after VO1	t_{DELAY}		4.2		
VO3 Start-Up Time	t_{SS3}		1.5		
VO4 Start-Up Time	t_{SS4}		1.0		
VO5 Start-Up Time	t_{SS5}		1.0		

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		100	100	400		1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4		0.6		0.26		μs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		0.5		μs
High Period of SCL Clock	t_{HIGH}	4		0.6		0.26		μs
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4.7		0.6		0.26		μs
Data Setup Time	$t_{SU;DATA}$	250		100		50		ns
Data Hold Time	$t_{HD;DATA}$	0		0		0		μs
Rising Time of SCL Clock	t_{RCL}		1000	20	300		120	ns
Falling Time of SCL Clock	t_{FCL}		300		300		120	ns
Rising Time of SDA Clock	t_{RDA}		1000	20	300		120	ns
Falling Time of SDA Clock	t_{FDA}		300		300		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4		0.6		0.26		μs
Bus Free Time between a STOP and a START Condition	t_{BUF}	4.7		1.3		0.5		μs
Noise Margin at LOW	V_{nL}	0.1 × V_{VIO}		0.1 × V_{VIO}		0.1 × V_{VIO}		V
Noise Margin at HIGH	V_{nH}	0.2 × V_{VIO}		0.2 × V_{VIO}		0.2 × V_{VIO}		V
Pulse Width of Spikes must be Suppressed by the Input Filter	t_{SP}	0	50	0	50	0	50	ns
Data Valid Time	t_{VD_DAT}		3.45		0.9		0.45	μs
Data Valid Acknowledge Time	t_{VD_ACK}		3.45		0.9		0.45	μs

NOTE:
1. Industry standard I²C timing characteristics are according to I²C-Bus Specification. Not tested in production.

I²C INTERFACE TIMING DIAGRAM

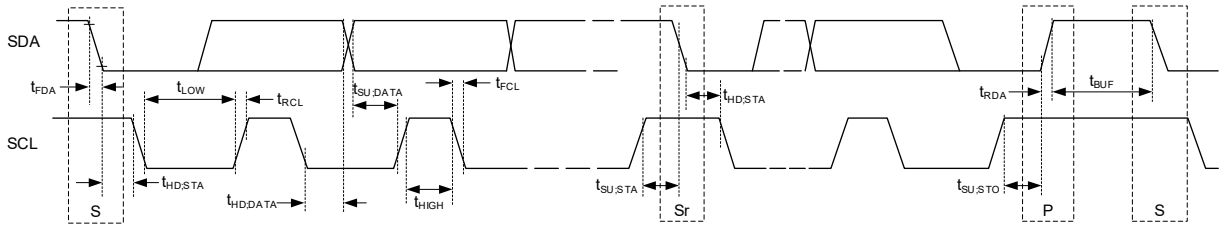
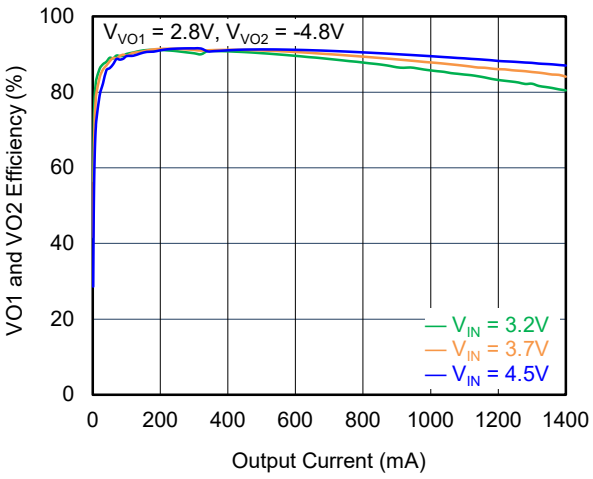


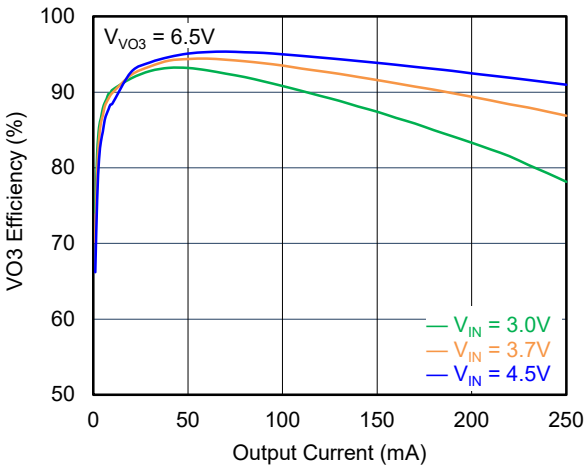
Figure 2. Serial Interface Timing for F/S-Mode

TYPICAL PERFORMANCE CHARACTERISTICS

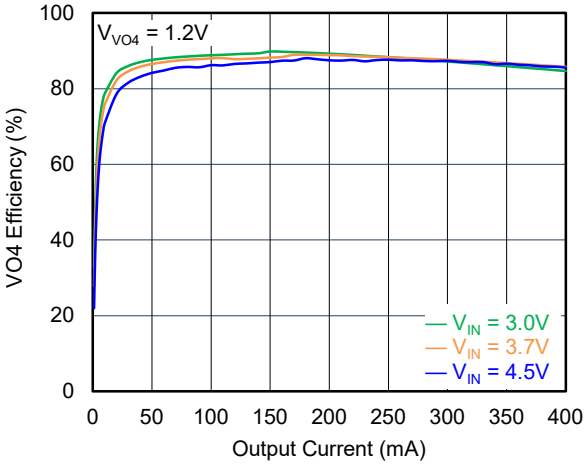
VO1 and VO2 Combined Efficiency vs. Output Current



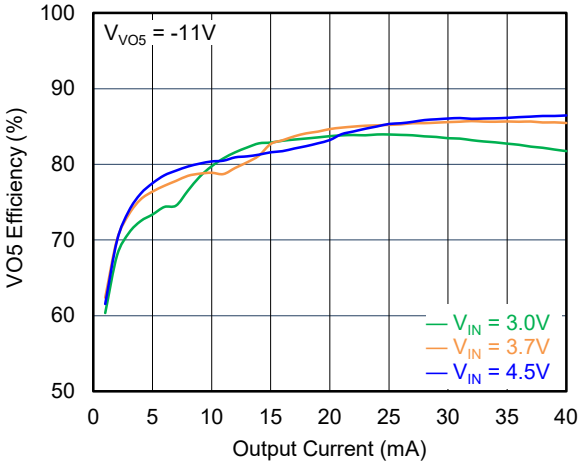
VO3 Efficiency vs. Output Current



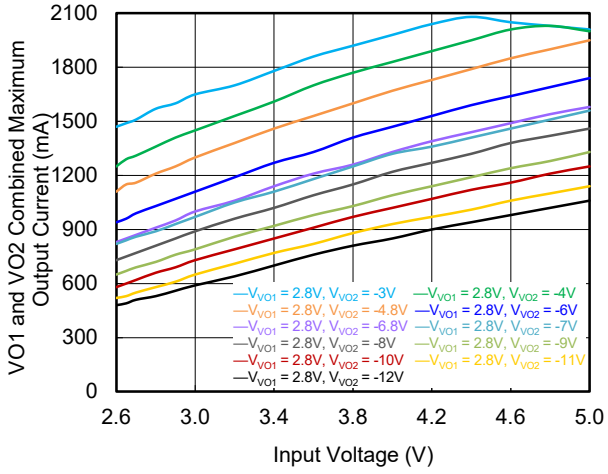
VO4 Efficiency vs. Output Current



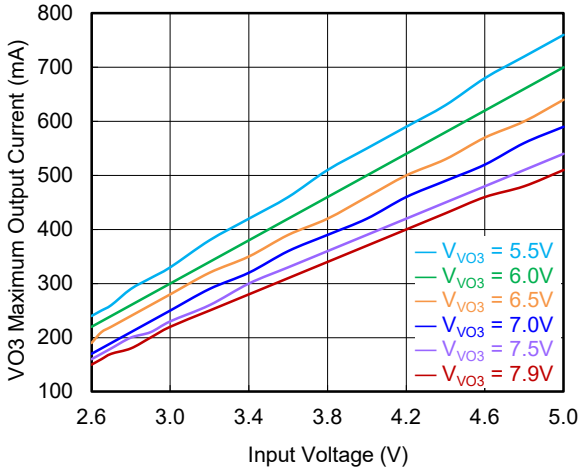
VO5 Efficiency vs. Output Current



VO1 and VO2 Combined Maximum Output Current vs. Input Voltage

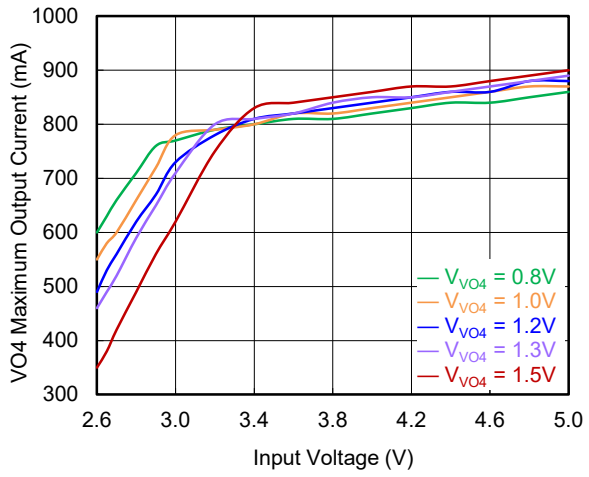


VO3 Maximum Output Current vs. Input Voltage

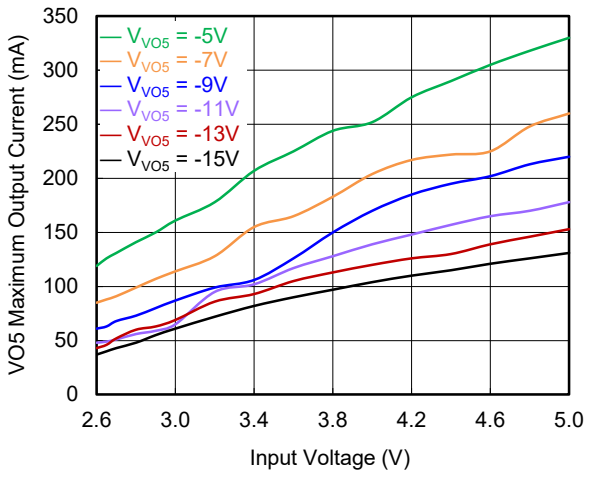


TYPICAL PERFORMANCE CHARACTERISTICS

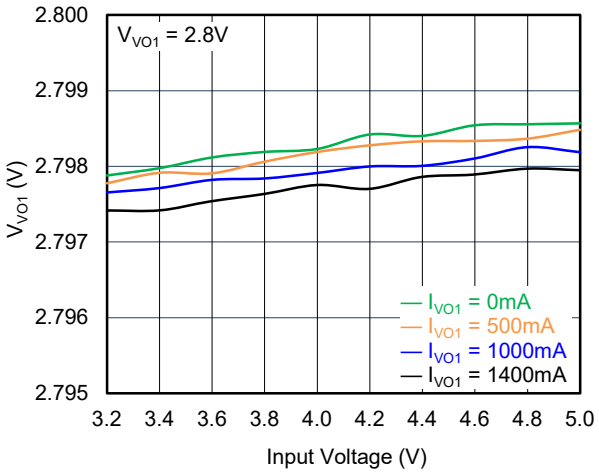
VO4 Maximum Output Current vs. Input Voltage



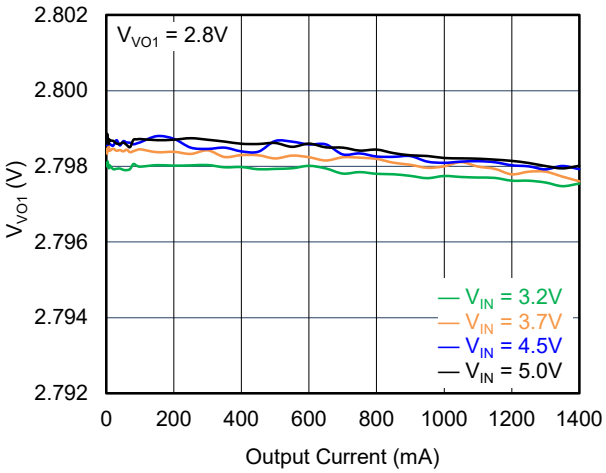
VO5 Maximum Output Current vs. Input Voltage



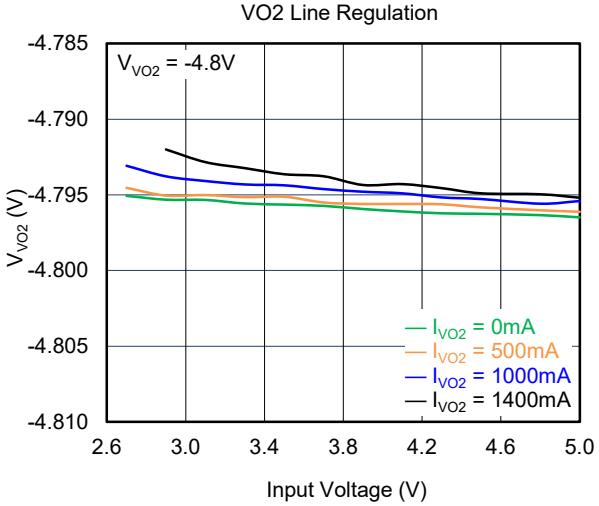
VO1 Line Regulation



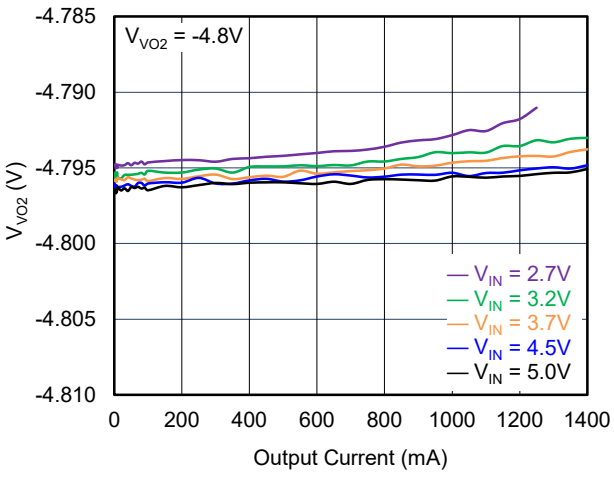
VO1 Load Regulation



VO2 Line Regulation

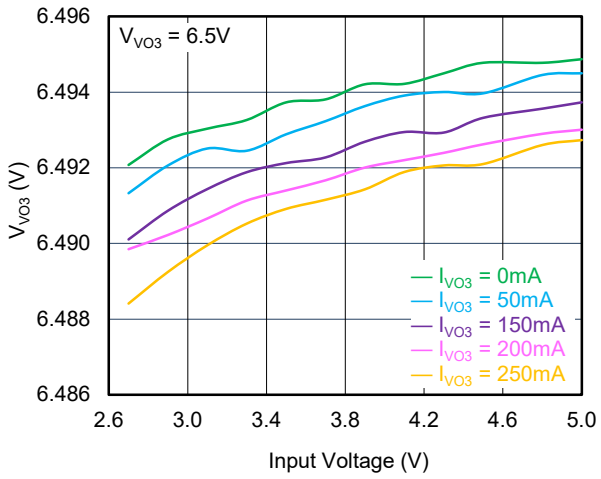


VO2 Load Regulation

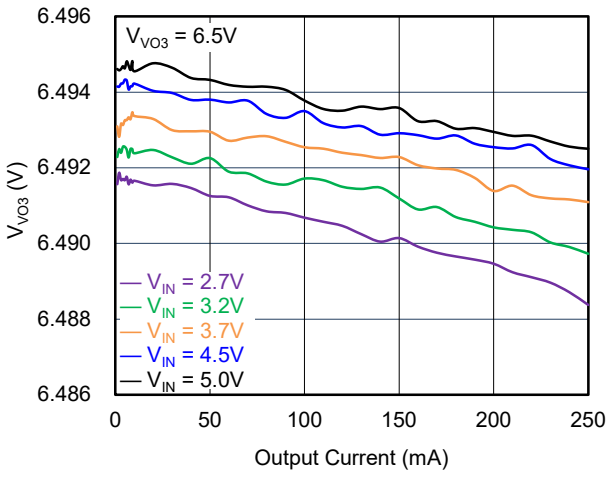


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

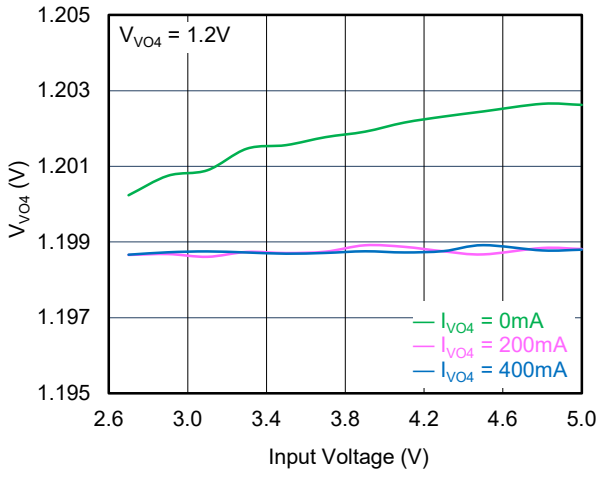
VO3 Line Regulation



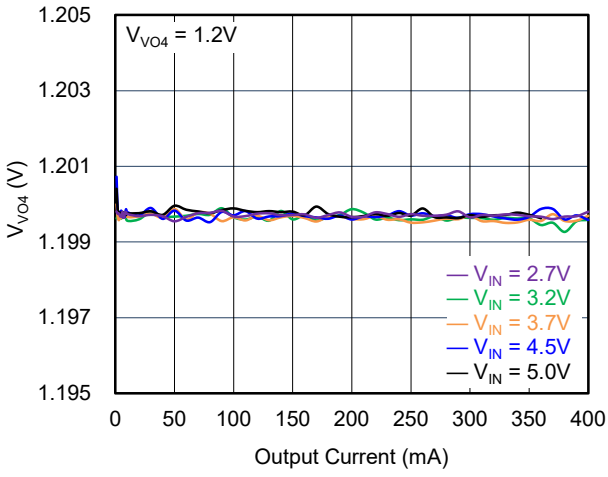
VO3 Load Regulation



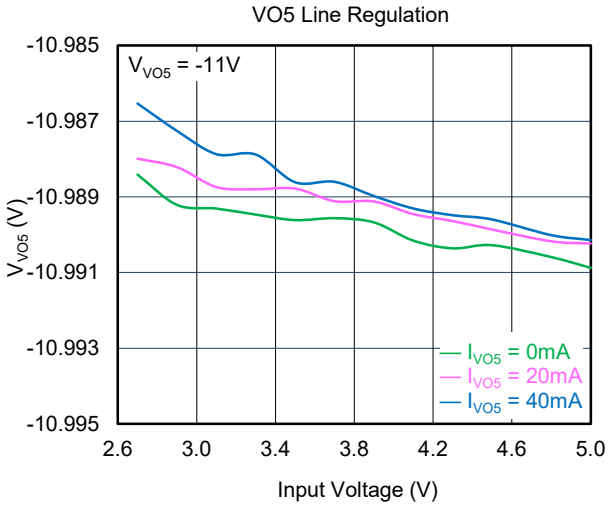
VO4 Line Regulation



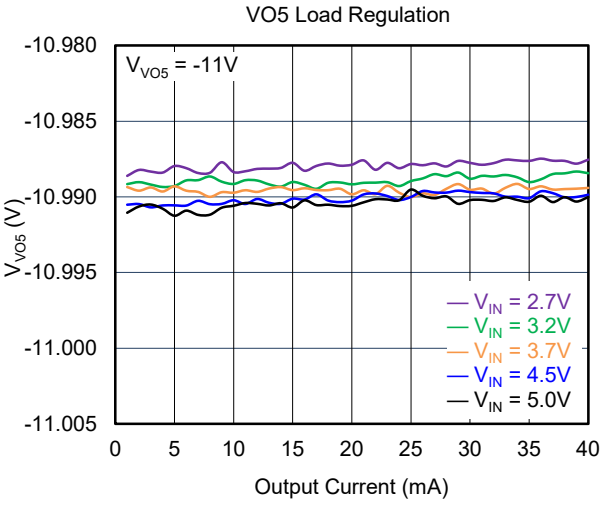
VO4 Load Regulation



VO5 Line Regulation

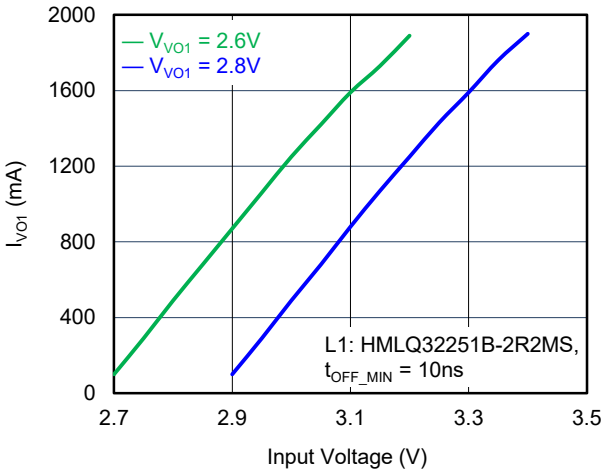


VO5 Load Regulation

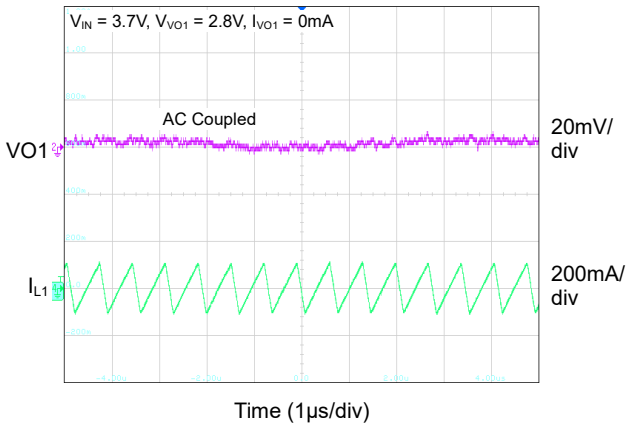


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

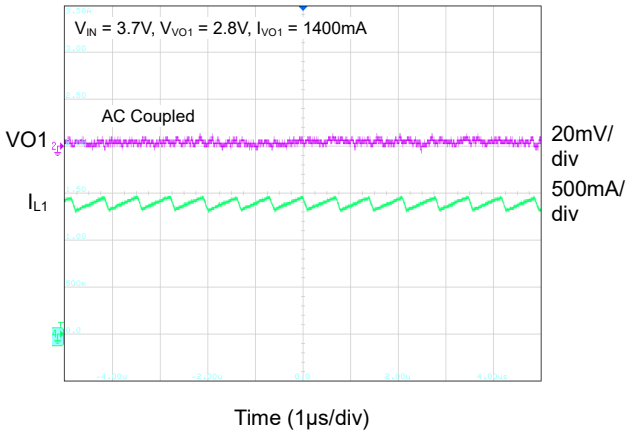
VO1 Maximum Output Current Capability at About 100% Duty



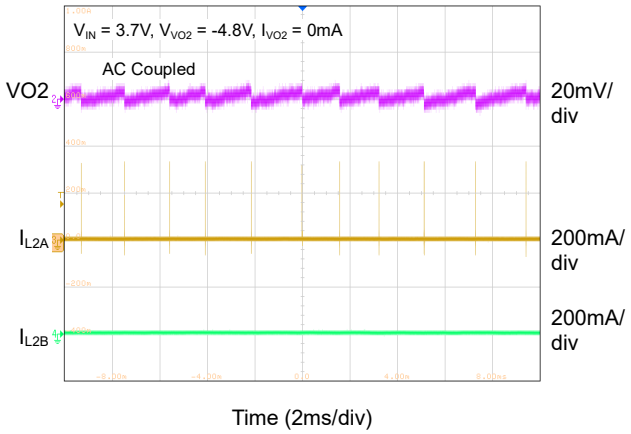
VO1 Output Voltage Ripple at No Load



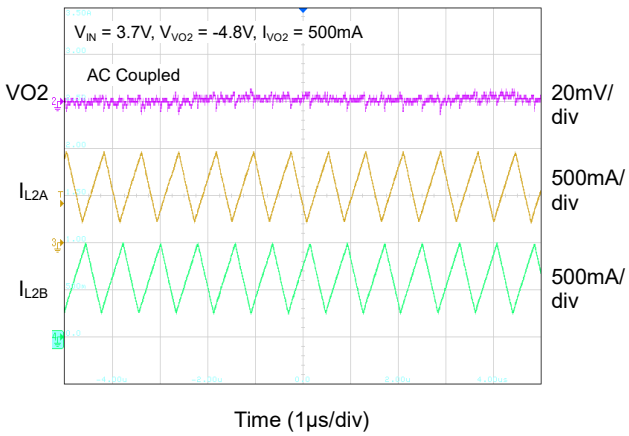
VO1 Output Voltage Ripple at Heavy Load



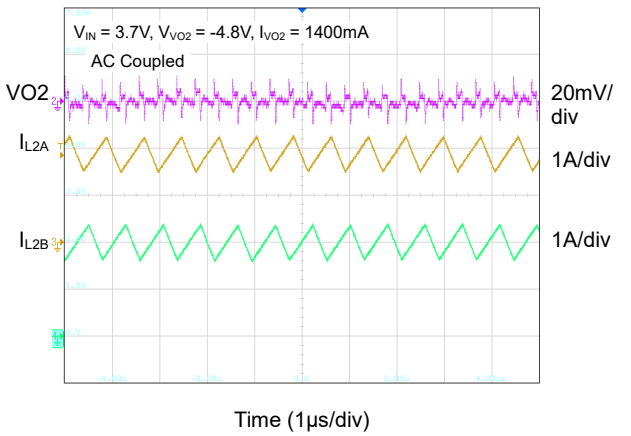
VO2 Output Voltage Ripple at No Load



VO2 Output Voltage Ripple at Moderate Load

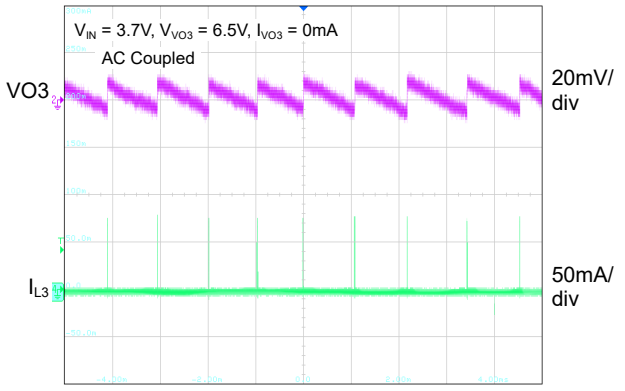


VO2 Output Voltage Ripple at Heavy Load

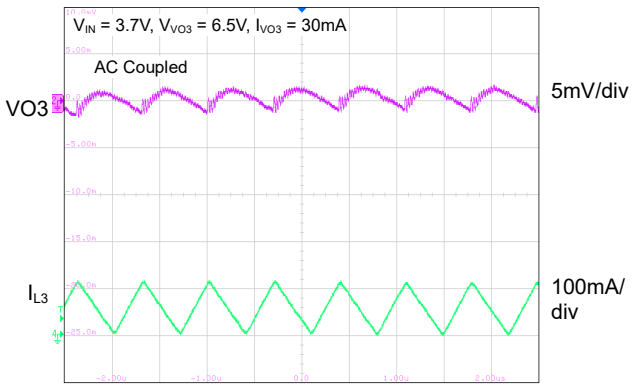


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

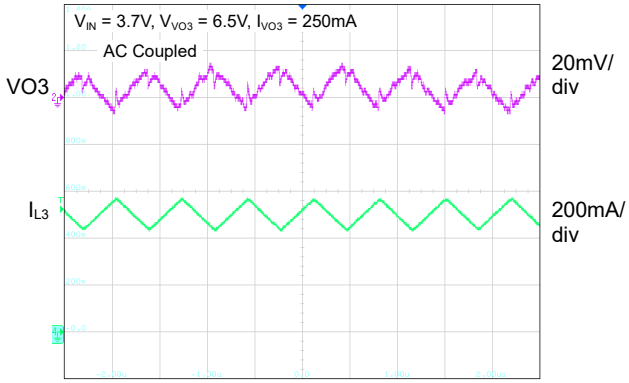
VO3 Output Voltage Ripple at No Load



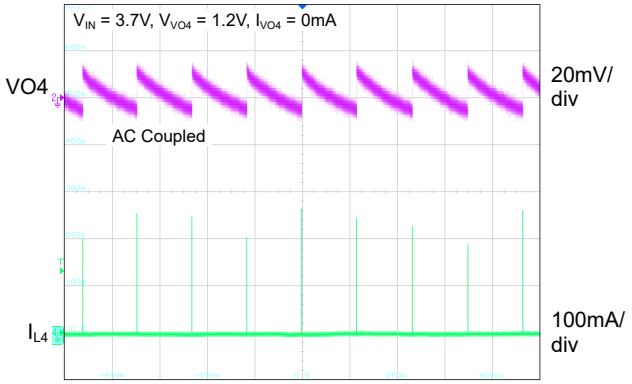
VO3 Output Voltage Ripple at Light Load



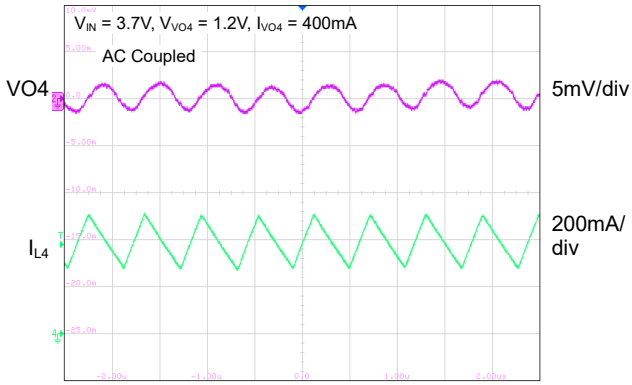
VO3 Output Voltage Ripple at Heavy Load



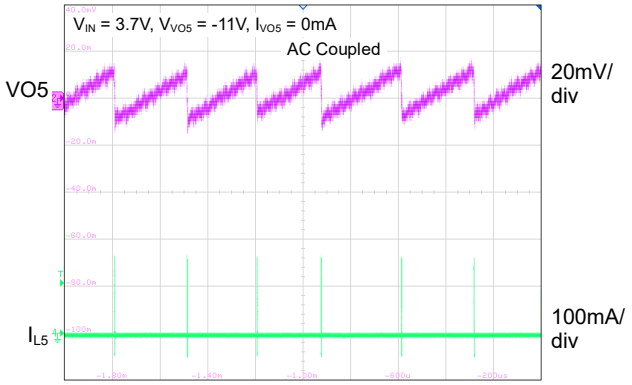
VO4 Output Voltage Ripple at Light Load



VO4 Output Voltage Ripple at Heavy Load

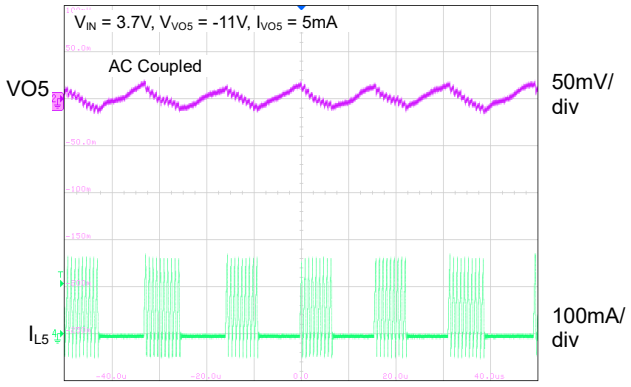


VO5 Output Voltage Ripple at No Load

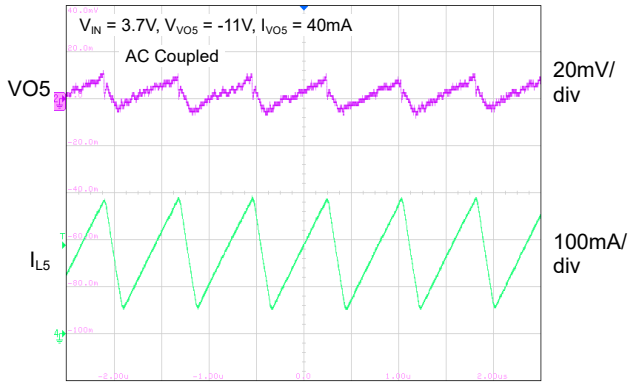


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

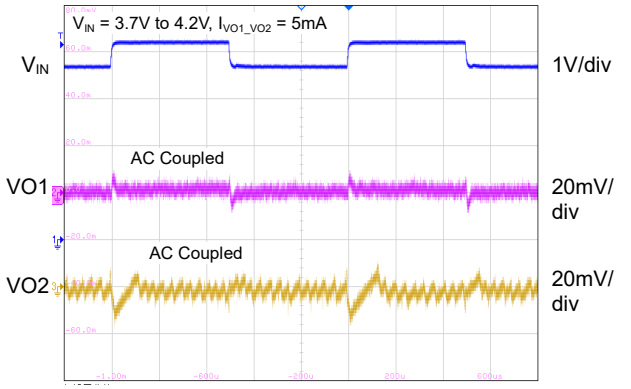
VO5 Output Voltage Ripple at Light Load



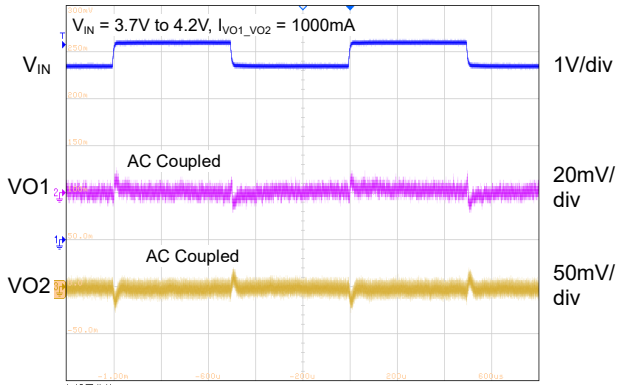
VO5 Output Voltage Ripple at Heavy Load



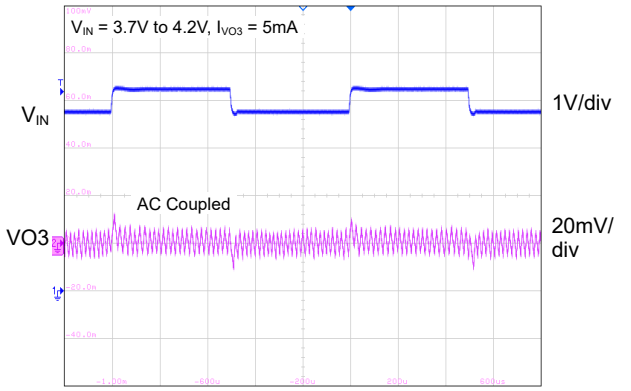
VO1 and VO2 Line Transient at Light Load



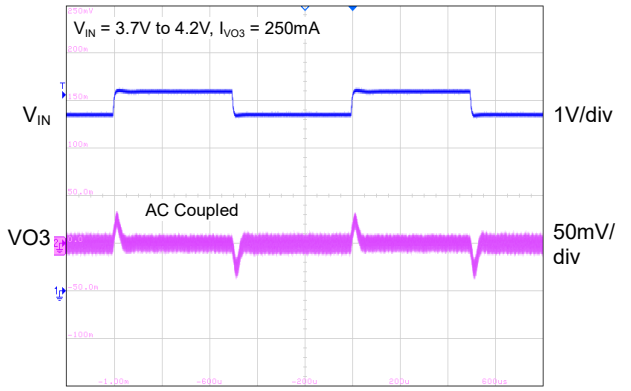
VO1 and VO2 Line Transient at Heavy Load



VO3 Line Transient at Light Load

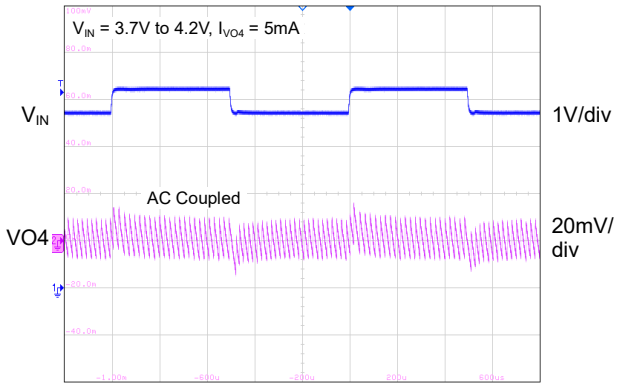


VO3 Line Transient at Heavy Load

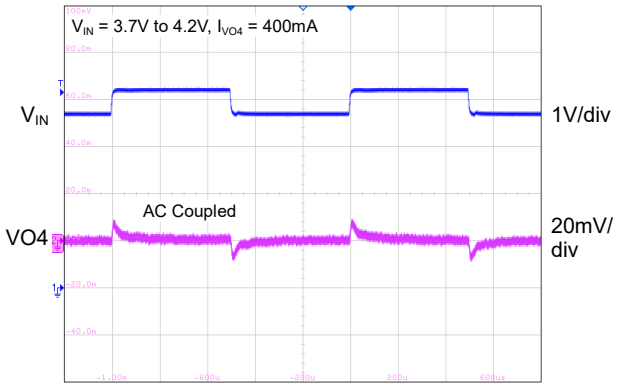


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

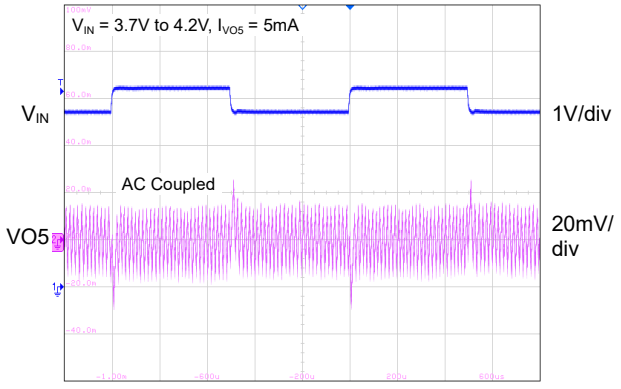
VO4 Line Transient at Light Load



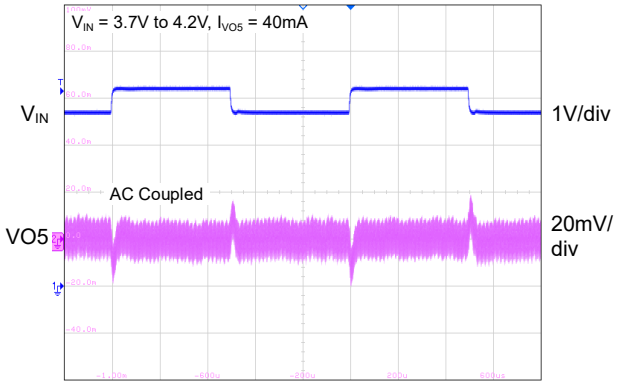
VO4 Line Transient at Heavy Load



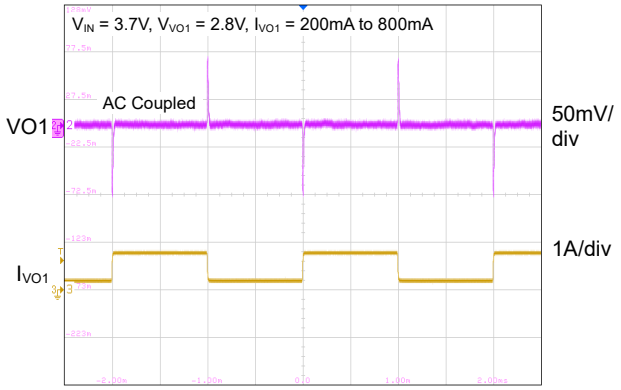
VO5 Line Transient at Light Load



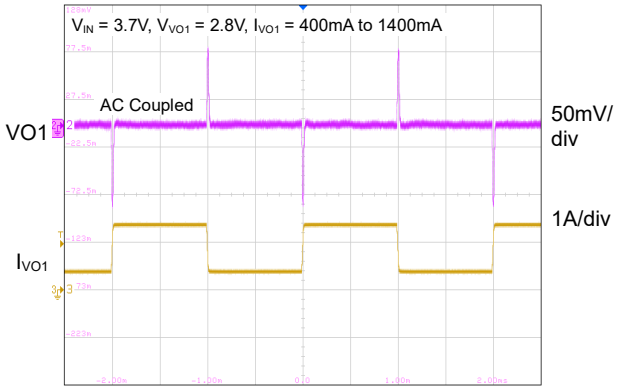
VO5 Line Transient at Heavy Load



VO1 Load Transient

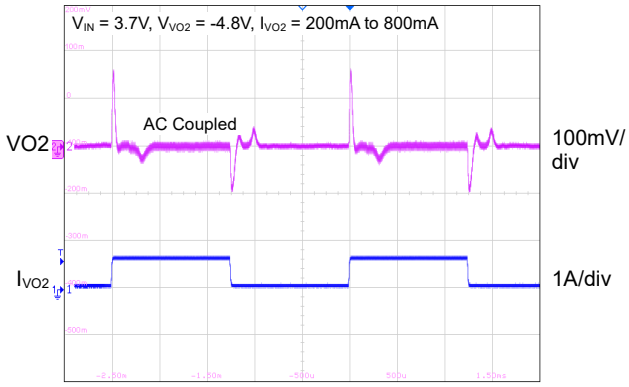


VO1 Load Transient



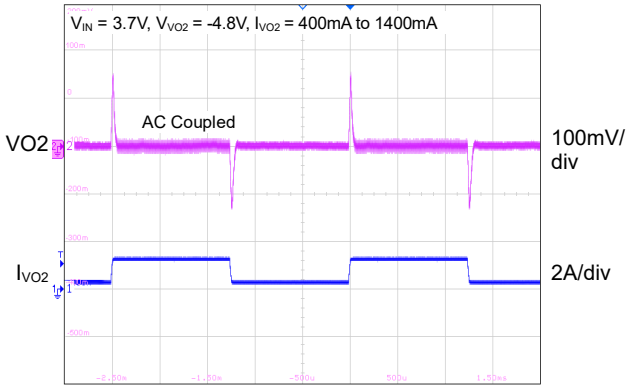
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO2 Load Transient



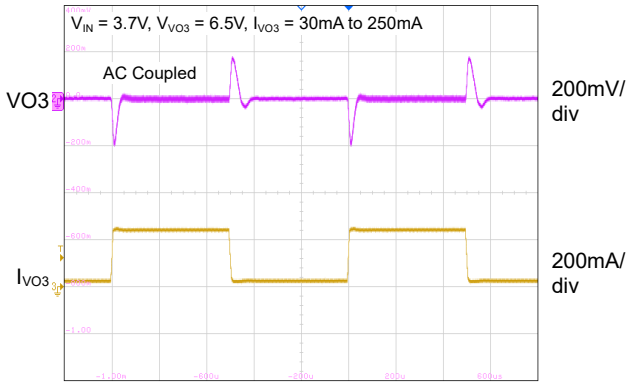
Time (500μs/div)

VO2 Load Transient



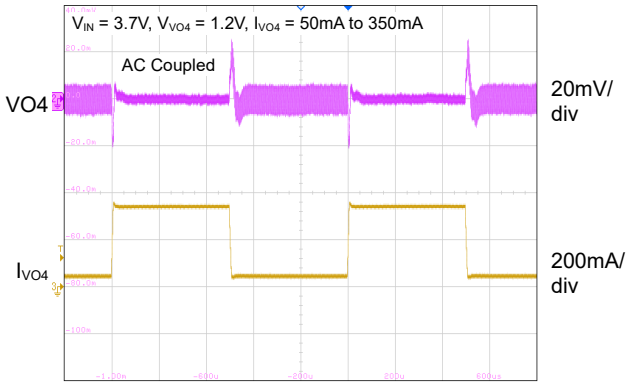
Time (500μs/div)

VO3 Load Transient



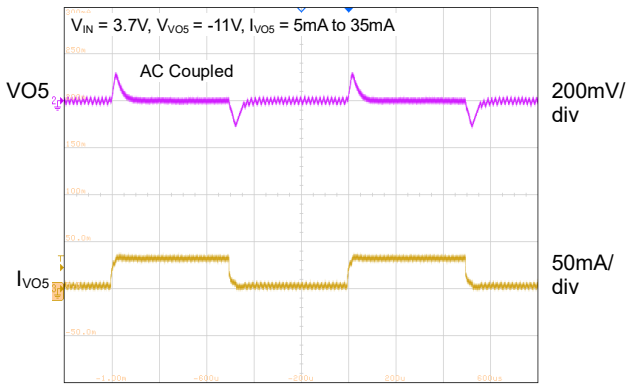
Time (200μs/div)

VO4 Load Transient



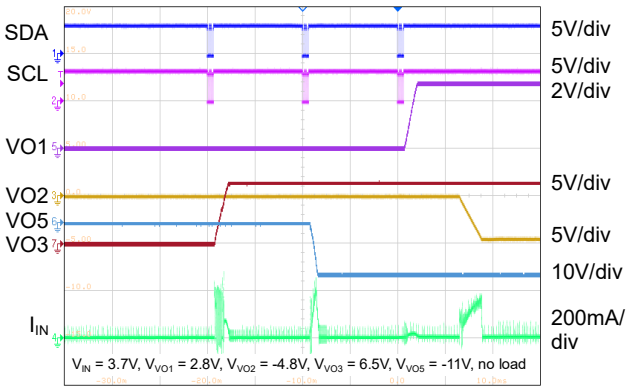
Time (200μs/div)

VO5 Load Transient



Time (200μs/div)

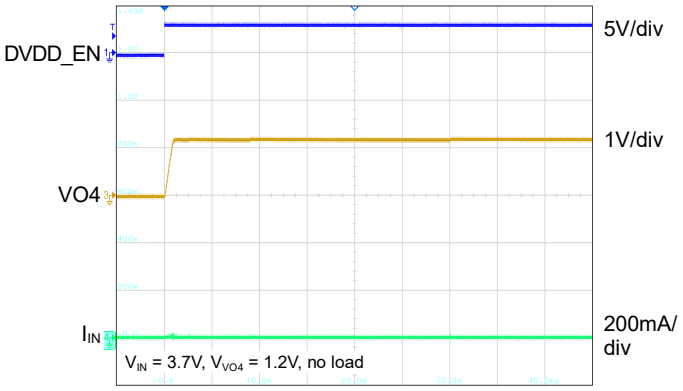
Start-Up Sequence



Time (5ms/div)

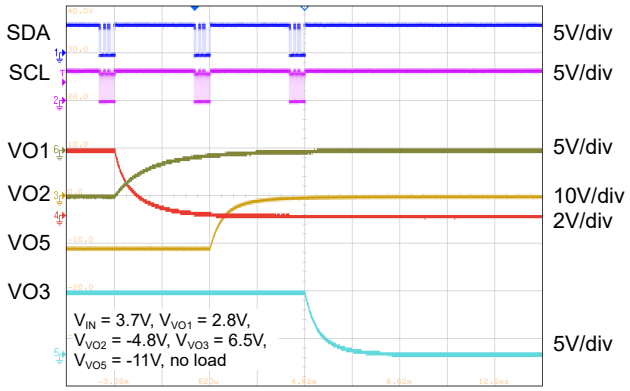
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Start-Up Sequence



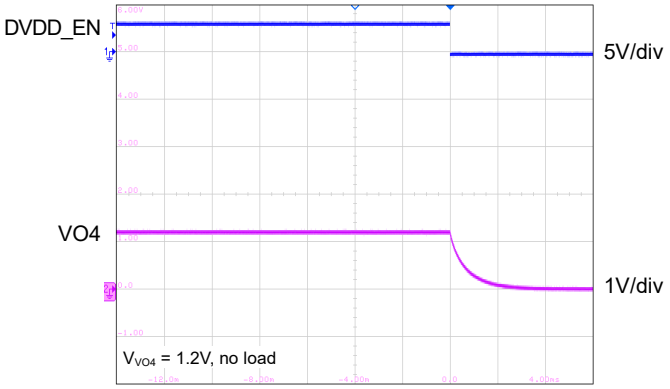
Time (5ms/div)

Shutdown Sequence Discharge = ON



Time (2ms/div)

Shutdown Sequence Discharge = ON



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

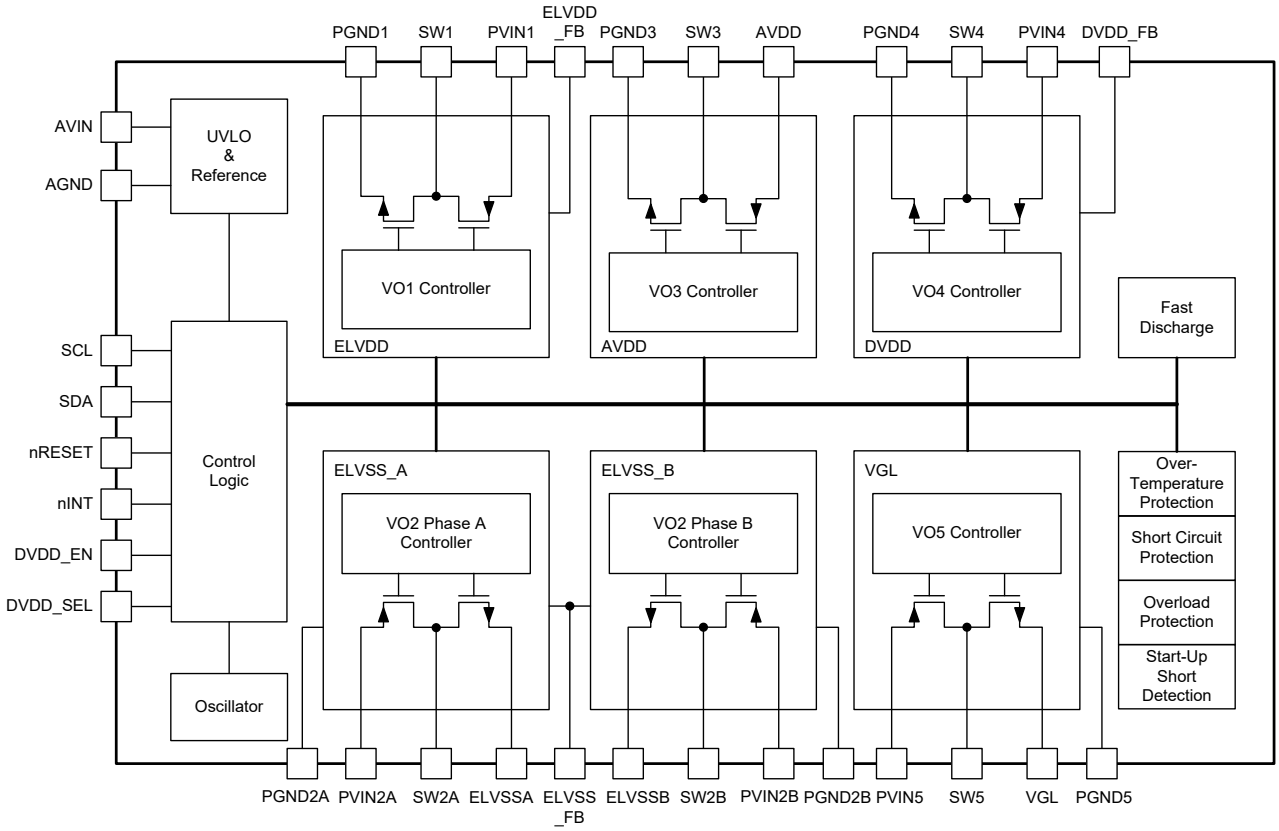


Figure 3. Functional Block Diagram

TIMING DIAGRAM

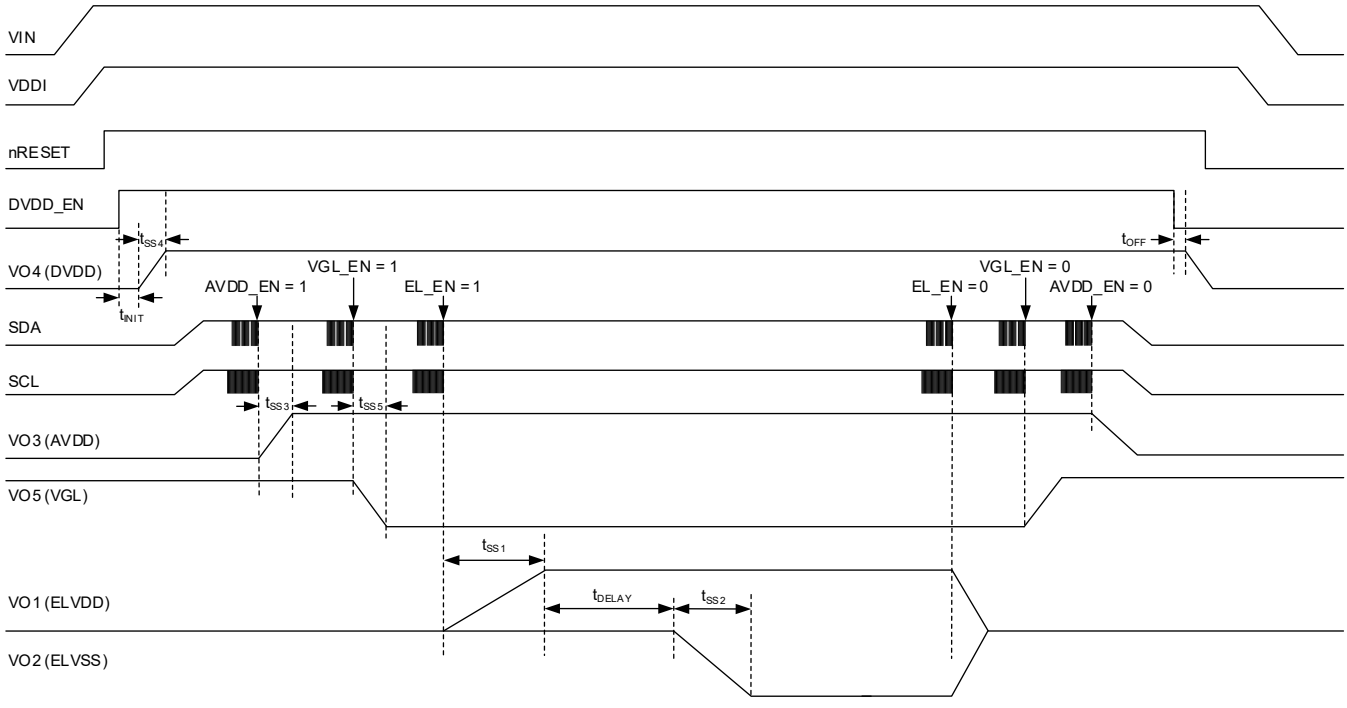


Figure 4. Timing Diagram

DETAILED DESCRIPTION

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down all the outputs when the junction temperature exceeds +150℃ (TYP), and restarts with the same programmed voltages and sequences when the temperature decreases to +135℃ (TYP).

Buck Converter VO1 (ELVDD)

The Buck converter VO1 operates with a peak-current-mode topology. The VO1 output voltage can be programmed between 2V and 3V (default 2.8V) with 100mV steps (see ELVDD_SET register).

The output sense pin (ELVDD_FB) is always connected to the positive pin of output capacitor for the highest output voltage accuracy.

Inverting Buck-Boost Converter VO2 (ELVSS)

The inverting Buck-Boost converter VO2 operates with a peak-current-mode topology and dual-phase fixed 1.25MHz (TYP) frequency. The VO2 output voltage can be programmed between -2V and -12V (default -4.8V) with 50mV steps (see ELVSS_SET register).

When the load current exceeds 340 TIMING DIAGRAM mA, phase A and phase B of the inverting Buck-Boost converter both work. And only phase A works when the load current decreases to 240mA for reducing the switching loss.

The output of VO2 is fully isolated in shutdown mode.

Boost Converter VO3 (AVDD)

The Boost converter VO3 operates with a peak-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO3 output voltage can be programmed between 5.5V and 7.9V (default 6.5V) with 100mV steps (see AVDD_SET register).

The output of VO3 is fully isolated in shutdown mode.

Buck Converter VO4 (DVDD)

The Buck converter VO4 operates with an adaptive COT (constant on time) mode topology. The VO4 output voltage can be programmed between 0.8V and 1.5V with 10mV steps (see DVDD_SET register). The default value can be set to 1.0V, 1.2V, and 1.3V by setting DVDD_SEL pin high, low, and leaving this pin floating, respectively.

Inverting Buck-Boost Converter VO5 (VGL)

The inverting Buck-Boost converter VO5 operates with a peak-current-mode topology and fixed 1.25MHz (TYP) frequency. The VO5 output voltage can be programmed between -5V and -15V (default -11V) with 100mV steps (see VGL_SET register).

The output of VO5 is fully isolated in shutdown mode.

Soft-Start, Start-Up, Discharge and Shutdown

The built-in soft-start function is adopted to limit the inrush current.

Writing EL_EN bit enables the VO1 Buck converter. VO1 starts with a 0.95A until soft-start current limit until it rises to the programmed voltage. Then the full current limit is active (2.3A, TYP).

5.7ms after writing 1 to EL_EN bit, the VO2 converter starts switching phase A (VO2A) with a 0.7A current limit until the VO2 rises to the default voltage (-4.8V). Then the full current limit is active (3.5A per phase, TYP).

Writing AVDD_EN bit enables the VO3 Boost converter. Before VO3 rises to the default value (6.5V), it rises linearly for 1.5ms with a 0.35A current limit. Then the full current limit is active (1.35A, TYP).

Toggling DVDD_EN high starts the VO4 Buck converter. Before VO4 rises to the default value (1.0V/1.2V/1.3V), it rises linearly for 1ms with a 0.9A current limit. Then the full current limit is active (1A, TYP).

Writing VGL_EN bit starts the VO5 Buck-Boost inverting converter. Before VO5 rises to the default value (-11V), it rises linearly for 1ms with a 0.6A current limit. Then the full current limit is active (1A, TYP).

The output discharge function can be controlled by the fast discharge control bits (*_FD_EN) in FD_CTRL register.

DETAILED DESCRIPTION (continued)

Short Circuit and Overload Protection

The device is protected from damage of all the converters shorting to ground. The device is also protected when V_{ELVDD} and V_{ELVSS} are shorted together during start-up.

A short at anyone of V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} can shut down all the four converters, then the shutdown state is latched, and the input is fully disconnected with these outputs.

A short between V_{ELVDD} and V_{ELVSS} during startup can shut down the V_{ELVDD} and V_{ELVSS} converters, then the shutdown state is latched, and the input is fully disconnected with these outputs. The Start-Up Short Detection (SSD) function can be controlled by the SSD_EN control bit in FD_CTRL register.

A short at V_{DVDD} can shut down the V_{DVDD} converter. Then the shutdown state is latched, and the input is fully disconnected with the output.

The device detects a short or an overload when one of the below conditions is fulfilled:

- V_{ELVDD} is not in regulation 2.5ms after V_{ELVDD} is enabled then all converters shut down.
- V_{ELVSS} is not in regulation 6.7ms after V_{ELVSS} is enabled then all converters shut down.
- V_{AVDD} protection is enabled when the soft-start is completed.
- V_{DVDD} protection is enabled when the soft-start is completed.
- V_{VGL} protection is enabled when the soft-start is completed.

- V_{ELVDD} falls below 82% of the programmed output voltage longer than 1ms during buck mode, then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.
- V_{ELVSS} rises above 87% of the programmed output voltage longer than 1ms then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.
- V_{AVDD} falls below 89% of the programmed output voltage longer than 1ms then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.
- V_{DVDD} falls below 87% of the programmed output voltage longer than 1ms then it shuts down.
- V_{VGL} rises above 82% of the programmed output voltage longer than 1ms then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.

Device Reset

The device has a global enable/reset control pin nRESET. nRESET must be pulled to high during operation.

In order to reset the whole device, V_{IN} has to cycle below digital UVLO (1.8V, TYP), or toggling nRESET low for minimum t_{RST} (20μs, TYP).

Once toggling nRESET low for t_{RST}, all the outputs shut down, all registers reset, and all latch-off states lift.

- A power cycle resets all settings to default values.
- Short circuit at one of the V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} resets all the four converters' settings.
- Short circuit at V_{DVDD} resets V_{DVDD} converter's setting.
- Pulling nRESET low for t_{RST} then short circuit protection is reset.
- Pulling nRESET low for t_{RST} then all the converter settings are reset.
- Writing EL_EN = 0 resets the output voltage of ELVDD and ELVSS.
- Writing AVDD_EN = 0 resets the output voltage of AVDD.
- Writing DVDD_EN = 0 or toggling DVDD_EN low for t_{OFF} resets the output voltage of DVDD.
- Writing VGL_EN = 0 resets the output voltage of VGL.

Output Current Capacity

The device operates with an input voltage range of 3.0V to 5.0V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage (above UVLO) or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 3.0V and 5.0V. To achieve full performance, a stable and noise-free input source is needed. Once the distance between input source and SGM3852 is a bit long, additional capacitors are suggested to place as close to the device as possible. Please refer to the typical application circuit for the suggested input capacitance.

DETAILED DESCRIPTION (continued)

Table 2. Device Control Logic

Conditions				COM	Register Status			DC/DC Control		Fast Discharge	
MODE	Input Voltage	nRESET	DVDD_EN	I²C	FLAG_REG	STAT_REG	OTHER_REG	EL/AVDD/VGL	DVDD	DVDD_FD	OTHER_FD
INVALID_POWER	< 1.8V	X	X	NA	NA	NA	NA	NA	NA	NA	NA
UVLO	1.8V ~ 2.45V	L	X	NA	FREEZE	DEFAULT	DEFAULT	NA	NA	ON	ON
		H	X	READ Only	ACTIVE	ACTIVE		NA	NA	ON	ON
SLEEP	> 2.45V	L	X	NA	FREEZE	DEFAULT	DEFAULT	NA	NA	ON	ON
NORMAL	> 2.45V	H	H	ACTIVE	ACTIVE	ACTIVE	ACTIVE	REG CTRL	ON	OFF	REG CTRL
			L						OFF	REG CTRL	

nINT Interrupt Output Pin

When a new update occurs in the device states, a 180μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the device and by receiving the interrupt it can react and check the situation on time.

The faults reflected in FAULT_FLAG register can generate an interrupt pulse.

Once a fault/flag happens, the nINT pulse is asserted, and the status bits and fault/flag bits are updated in FAULT_STAT and FAULT_FLAG registers.

Fault/flag status is not reset in the register until the host reads it.

When a FLAG register is not cleared, the same interrupt event of status occurs again, and FLAG is maintained as 1, and a nINT pulse will still be generated.

Continuous interrupt: consists of single interrupt with at least 180μs blocking time between pluses. nINT should not be kept low.

When a continuous interrupt event occurs, if a new interrupt event occurs in the nINT pulse process, nINT pluse is no longer triggered. If a new interrupt event occurs within blocking time, then nINT pulse is generated after blocking time.

Therefore, in order to read the current time faults, the host must read FAULT_FLAG register two times consecutively. The first read returns the history of the fault register status (from the time of the last read or reset) and the second one checks the current active faults.

All interrupt events can be masked by MASK register. After MASK bit is set to 1, the corresponding status bit and Flag bit still work normally and no longer trigger interrupt nINT pulse.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3852 parameters and get status reports. I²C is well known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3852 operates as a slave device with address 0x66 (66H). It has fifteen 8-bit registers.

Physical Layer

The SGM3852 supports I²C standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (up to 1000kbit/s) communication speeds. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 5. All transactions begin by the master that applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

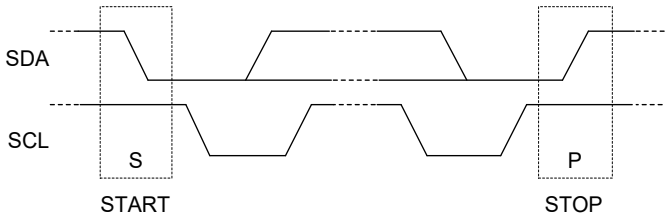


Figure 5. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the HIGH period of the clock. The state of the SDA can only change when the clock (SCL) is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 6.

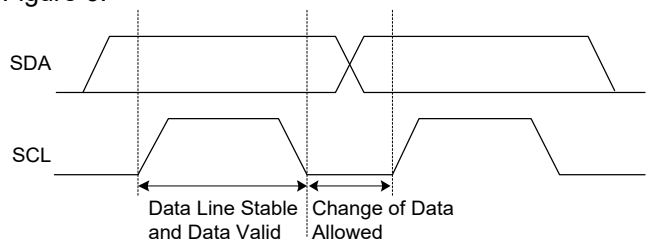


Figure 6. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 7 shows the byte transfer process with I²C interface.

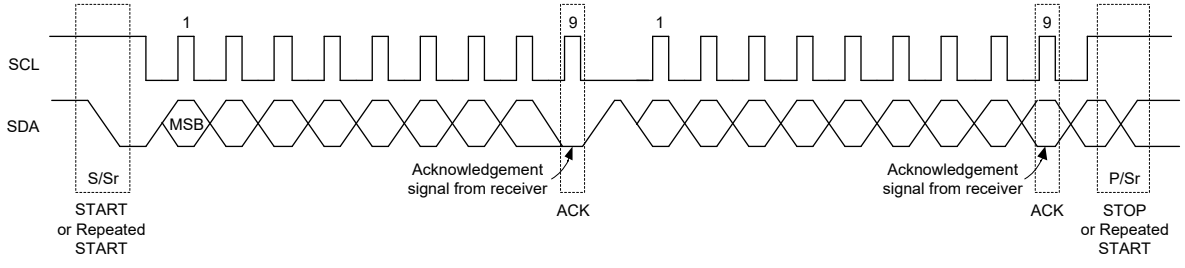


Figure 7. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)
After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte was received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge clock pulse. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address and then without a stop condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves
The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accesses in the next byte(s). The data transfer transaction is shown in Figure 8.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 9 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 10), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

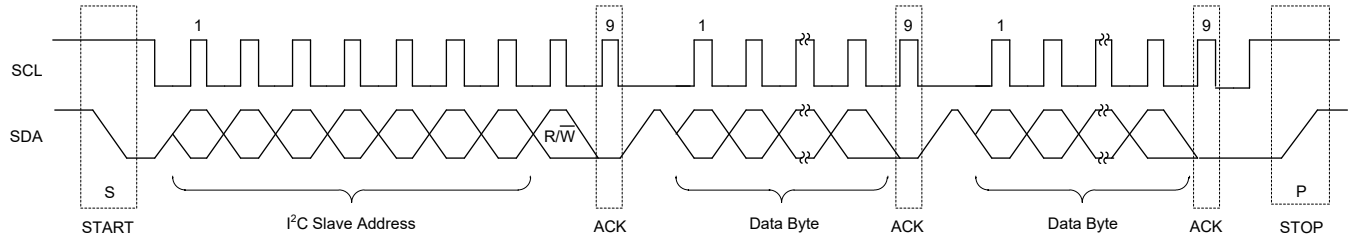


Figure 8. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

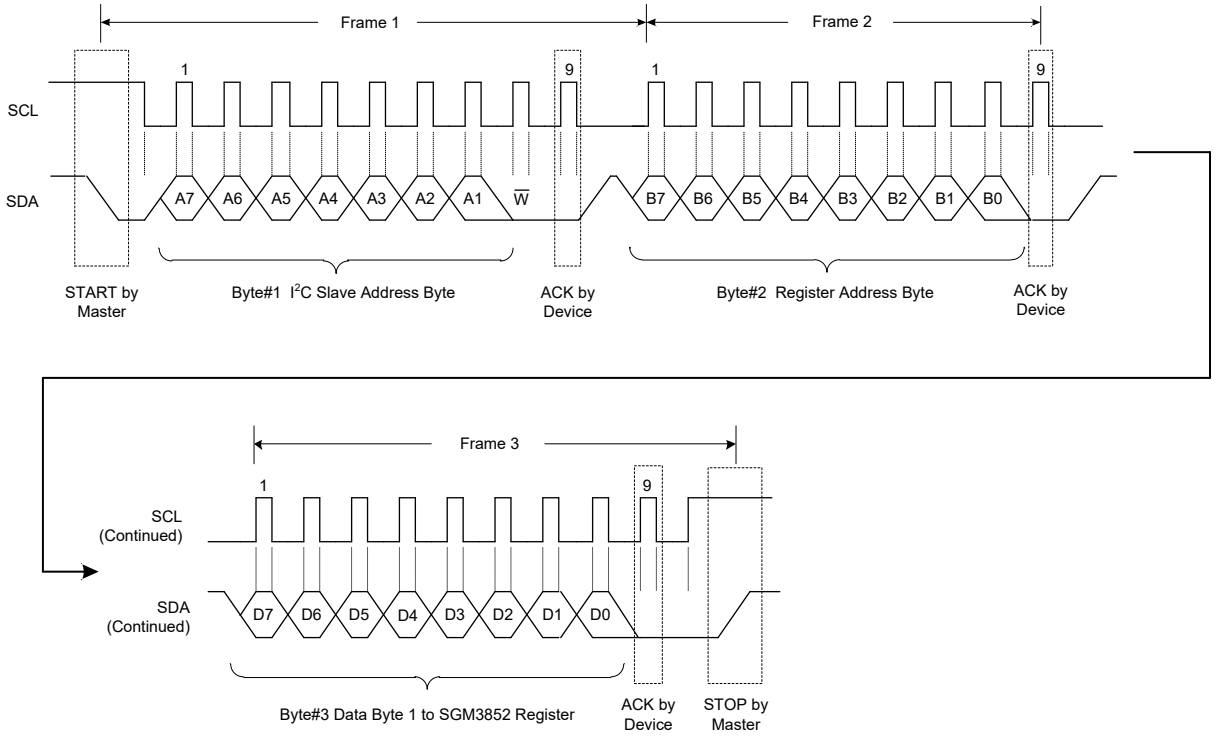


Figure 9. A Single Write Transaction

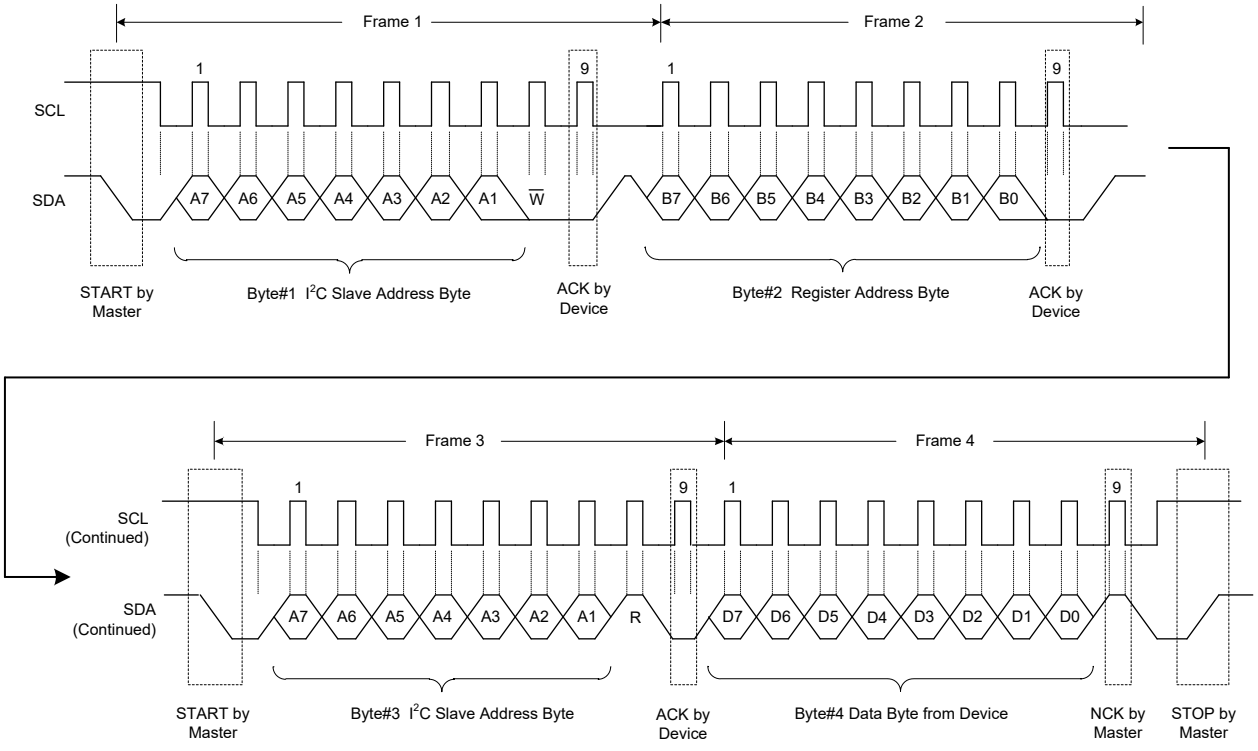


Figure 10. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3852 for REG0x00 through REG0x0E registers, except for REG0x06, as explained in Figure 11 and Figure 12. REG0x06 (FAULT_FLAG register) is skipped in multi-read/writes. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

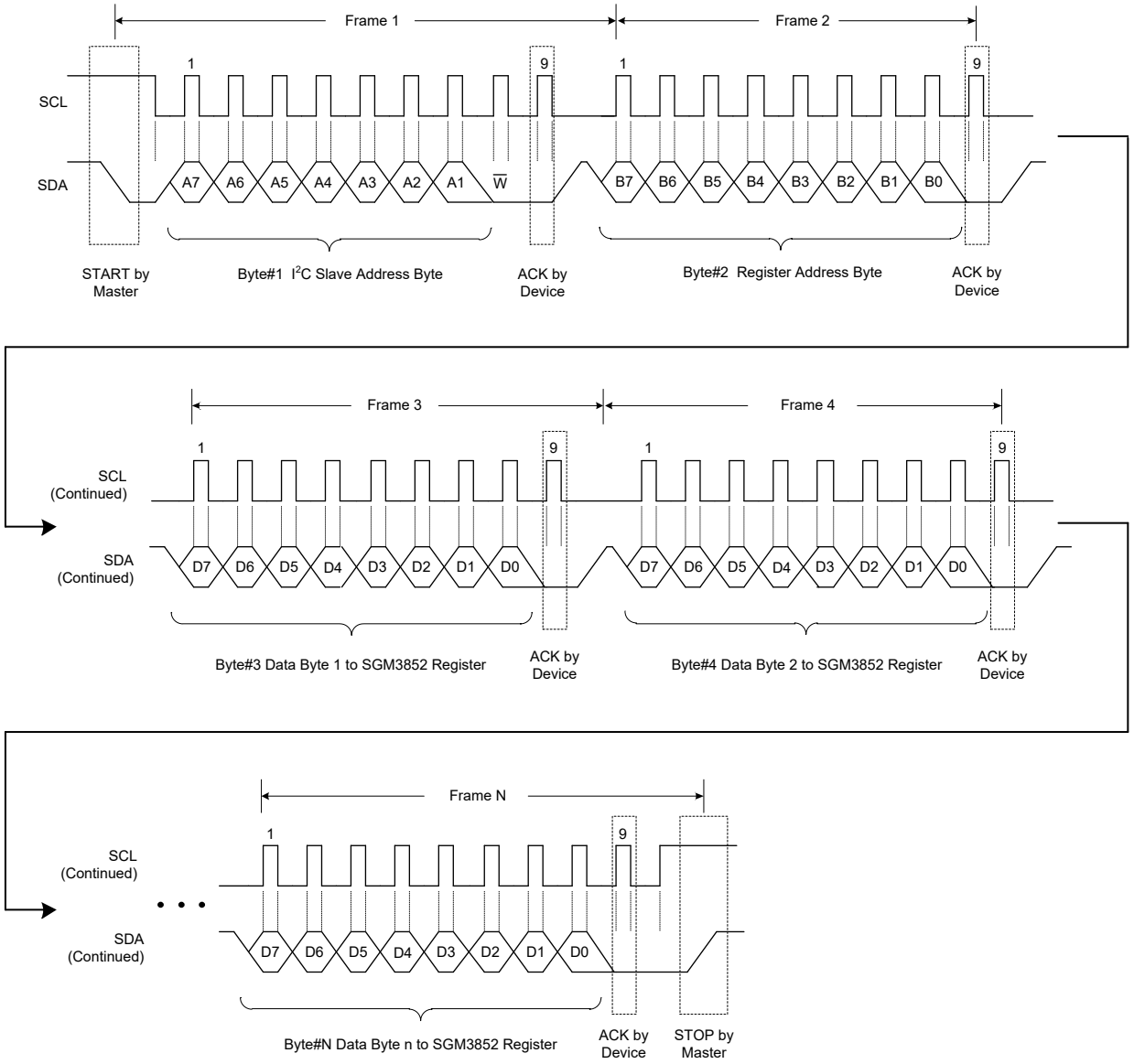


Figure 11. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

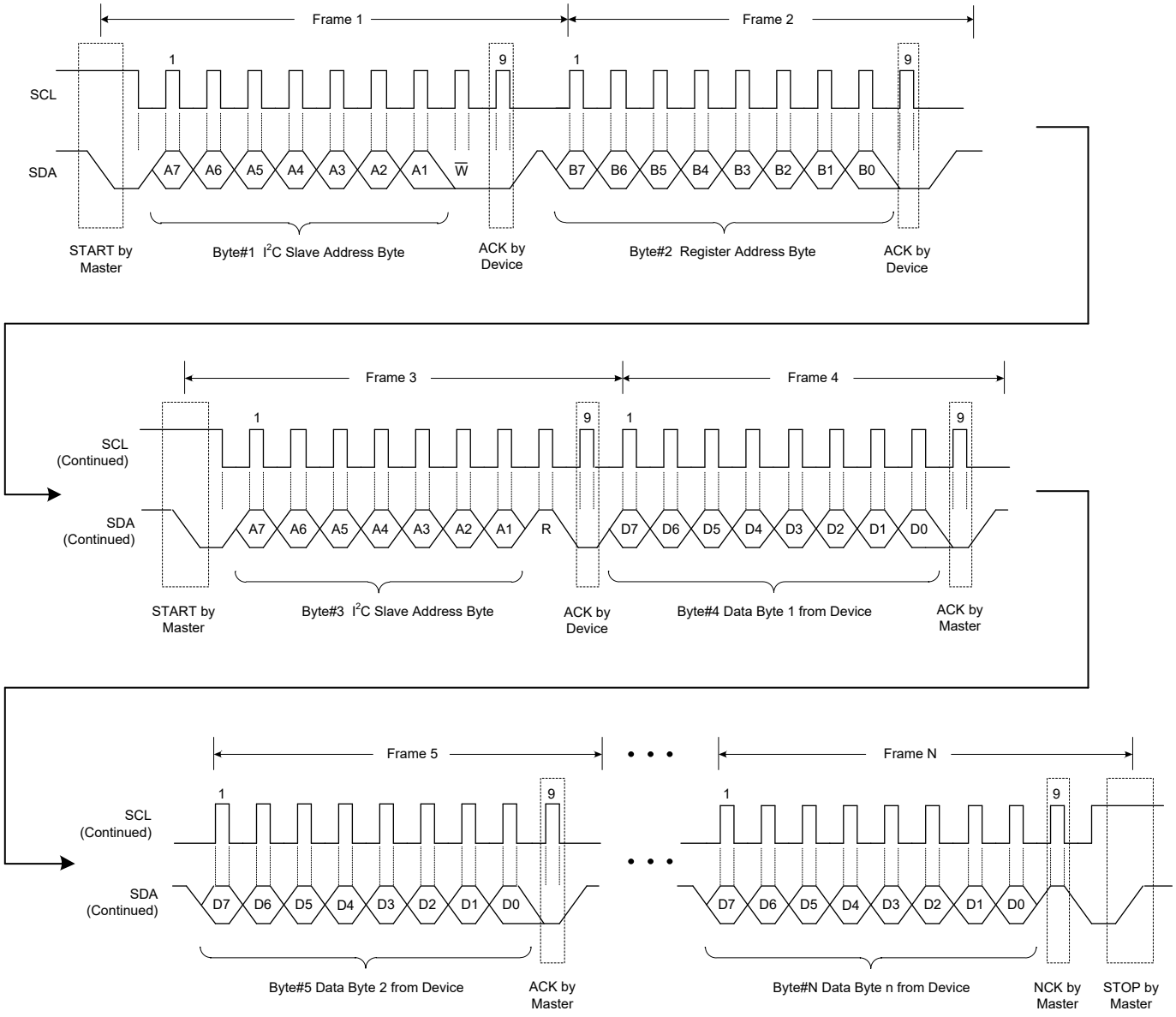


Figure 12. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM3852: 0x66 (1100110+ W/R, write 0xCC, read 0xCD)

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE							
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
POWR_ONOFF	0x00	Reserved			EN_AOD	Reserved	VGL_EN	AVDD_EN	EL_EN
		0	0	0	0	0	0	0	0
SYS_CTRL	0x01	Reserved		ELVSS_FSW[1:0]		FPWM_DVDD_EN	FPWM_ELVDD_EN	ELVSS_OP_SET[1:0]	
		0	0	0	0	0	1	0	0
FD_CTRL	0x02	Reserved		SSD_EN	VGL_FD_EN	DVDD_FD_EN	AVDD_FD_EN	ELVSS_FD_EN	ELVDD_FD_EN
		0	0	0	1	1	1	1	1
SR_CTRL	0x03	Reserved						ELVSS_SR[1:0]	
		0	0	0	0	0	0	0	0
PG_STAT	0x04	Reserved	VIN_POK	VGL_POK	DVDD_POK	AVDD_POK	ELVSS_POK	ELVDD_POK	POWER_GOOD
		0	0	0	0	0	0	0	0
FAULT_STAT	0x05	UVLO_STAT	EL_SSD_STATE	OTP_STATE	VGL_SCP_STATE	DVDD_SCP_STATE	AVDD_SCP_STATE	ELVSS_SCP_STATE	ELVDD_SCP_STATE
		0	0	0	0	0	0	0	0
FAULT_FLAG	0x06	UVLO_FLAG	EL_SSD_FLAG	OTP_FLAG	VGL_SCP_FLAG	DVDD_SCP_FLAG	AVDD_SCP_FLAG	ELVSS_SCP_FLAG	ELVDD_SCP_FLAG
		0	0	0	0	0	0	0	0
FAULT_MASK	0x07	UVLO_MASK	EL_SSD_MASK	OTP_MASK	VGL_SCP_MASK	DVDD_SCP_MASK	AVDD_SCP_MASK	ELVSS_SCP_MASK	ELVDD_SCP_MASK
		0	0	0	0	0	0	0	0
ELVDD_SET	0x08	Reserved				ELVDD_SET[3:0]			
		0	0	0	0	1	0	0	0
ELVSS_SET	0x09	ELVSS_SET[7:0]							
		0	0	1	1	1	0	0	0
AVDD_SET	0x0A	Reserved			AVDD_SET[4:0]				
		0	0	0	0	1	0	1	0
DVDD_SET	0x0B	Reserved	DVDD_SET[6:0] (DVDD_SEL = LOW)						
		0	0	1	0	1	0	0	0
VGL_SET	0x0C	Reserved	VGL_SET[6:0]						
		0	0	1	1	1	1	0	0
DEVICE_INFO	0x0D	PRODUCT_ID[3:0]				DEVICE_ID[3:0]			
		0	1	0	1	0	0	1	0
ELVSS_FREQ_SET	0x0E	Reserved			ELVSS_FREQ_SET[1:0]		Reserved		
		0	0	0	0	0	0	0	0
RESERVED	0x0F	Reserved							
		0	0	0	0	0	0	0	0

REGISTER MAP (continued)

Bit Types:
R: Read only
R/W: Read/Write

REG0x00: POWR_ONOFF Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	EN_AOD	0	R/W	Low Power Drive Mode for AOD (Always On Display) Control 0 = Disable (default) 1 = Enable
D[3]	Reserved	0	R/W	Reserved
D[2]	VGL_EN	0	R/W	VGL Output Control 0 = Disabled (default) 1 = Enabled
D[1]	AVDD_EN	0	R/W	AVDD Output Control 0 = Disabled (default) 1 = Enabled
D[0]	EL_EN	0	R/W	EL Output Control 0 = Disabled (default) 1 = Enabled

REG0x01: SYS_CTRL Register Address [reset = 0x04]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:4]	ELVSS_FSW[1:0]	00	R/W	ELVSS PWM Frequency control 00 = 1.5MHz (default) 01 = 1.2MHz 10 = 1.0MHz 11 = 0.8MHz
D[3]	FPWM_DVDD_EN	0	R/W	DVDD Forced PWM Mode Control 0 = Disabled (default) 1 = Enabled
D[2]	FPWM_ELVDD_EN	1	R/W	ELVDD Forced PWM Mode Control 0 = Disabled 1 = Enabled (default)
D[1:0]	ELVSS_OP_SET[1:0]	00	R/W	ELVSS Dual Phase Operation Mode Control 00 = Auto-mode (default) 01 = Auto-mode 10 = Single phase forced mode 11 = Reserved

REGISTER MAP (continued)

REG0x02: FD_CTRL Register Address [reset = 0x1F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5]	SSD_EN	0	R/W	EL Start-Up Short Detection Protection Control 0 = Disabled (default) 1 = Enabled
D[4]	VGL_FD_EN	1	R/W	VGL FD Function Control 0 = Disabled 1 = Enabled (default)
D[3]	DVDD_FD_EN	1	R/W	DVDD FD Function Control 0 = Disabled 1 = Enabled (default)
D[2]	AVDD_FD_EN	1	R/W	AVDD FD Function Control 0 = Disabled 1 = Enabled (default)
D[1]	ELVSS_FD_EN	1	R/W	ELVSS FD Function Control 0 = Disabled 1 = Enabled (default)
D[0]	ELVDD_FD_EN	1	R/W	ELVDD FD Function Control 0 = Disabled 1 = Enabled (default)

REG0x03: SR_CTRL Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	ELVSS_SR[1:0]	00	R/W	ELVSS Voltage Slew Rate Control Bit 00 = 50mV/50μs (default) 01 = 50mV/37.5μs 10 = 50mV/25μs 11 = 50mV/12.5μs

REG0x04: PG_STAT Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	VIN_POK	0	R	Power_GOOD Signal of VIN 0 = NG (default) 1 = OK
D[5]	VGL_POK	0	R	Power_GOOD Signal of VGL 0 = NG (default) 1 = OK
D[4]	DVDD_POK	0	R	Power_GOOD Signal of DVDD 0 = NG (Default) 1 = OK
D[3]	AVDD_POK	0	R	Power_GOOD Signal of AVDD 0 = NG (default) 1 = OK
D[2]	ELVSS_POK	0	R	Power_GOOD Signal of ELVSS 0 = NG (default) 1 = OK
D[1]	ELVDD_POK	0	R	Power_GOOD signal of ELVDD 0 = NG (default) 1 = OK
D[0]	POWER_GOOD	0	R	Power_GOOD of All the Enabled Rails 0 = NG (default) 1 = OK

REGISTER MAP (continued)

Table 3. Power Good Detection Threshold

Power	ELVDD	ELVSS	AVDD	DVDD	VGL
Output Voltage (V)	2 ~ 3	-2 ~ -12	5.5 ~ 7.9	0.8 ~ 1.5	-5 ~ -15
Rising (%)	85	90	90	90	90
Falling (%)	75	80	80	80	80
Hysteresis (%)	10	10	10	10	10
t_{RISING} (μs)	20	20	20	20	20
$t_{FALLING}$ (μs)	3	3	3	3	3

REG0x05: FAULT_STAT Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	UVLO_STAT	0	R	VIN UVLO Status 0 = VIN above UVLO 1 = VIN under UVLO
D[6]	EL_SSD_STATE	0	R	EL Start-Up Short Detection Event Status 0 = Normal 1 = EL SSD event happens
D[5]	OTP_STATE	0	R	Thermal shutdown Status 0 = Normal 1 = OTP event happens
D[4]	VGL_SCP_STATE	0	R	VGL Short Current Event Status 0 = Normal 1 = VGL SCP event happens
D[3]	DVDD_SCP_STATE	0	R	DVDD Short Current Event Status 0 = Normal 1 = DVDD SCP event happens
D[2]	AVDD_SCP_STATE	0	R	AVDD Short Current Event Status 0 = Normal 1 = AVDD SCP event happens
D[1]	ELVSS_SCP_STATE	0	R	ELVSS Short Current Event Status 0 = Normal 1 = ELVSS SCP event happens
D[0]	ELVDD_SCP_STATE	0	R	ELVDD Short Current Event Status 0 = Normal 1 = ELVDD SCP event happens

REGISTER MAP (continued)

REG0x06: FAULT_FLAG Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	UVLO_FLAG	0	R	VIN UVLO Event Interrupt 0 = Not trigger 1 = Triggered
D[6]	EL_SSD_FLAG	0	R	EL SSD Event Interrupt 0 = Not trigger 1 = Triggered
D[5]	OTP_FLAG	0	R	OTP Event Interrupt 0 = Not trigger 1 = Triggered
D[4]	VGL_SCP_FLAG	0	R	VGL SCP Event Interrupt 0 = Not trigger 1 = Triggered
D[3]	DVDD_SCP_FLAG	0	R	DVDD SCP Event Interrupt 0 = Not trigger 1 = Triggered
D[2]	AVDD_SCP_FLAG	0	R	AVDD SCP Event Interrupt 0 = Not trigger 1 = Triggered
D[1]	ELVSS_SCP_FLAG	0	R	ELVSS SCP Event Interrupt 0 = Not trigger 1 = Triggered
D[0]	ELVDD_SCP_FLAG	0	R	ELVDD SCP Event Interrupt 0 = Not trigger 1 = Triggered

REG0x07: FAULT_MASK Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	UVLO_MASK	0	R/W	VIN UVLO Event Interrupt Mask 0 = Not masked 1 = Masked
D[6]	EL_SSD_MASK	0	R/W	EL SSD Event Interrupt Mask 0 = Not masked 1 = Masked
D[5]	OTP_MASK	0	R/W	OTP Event Interrupt Mask 0 = Not masked 1 = Masked
D[4]	VGL_SCP_MASK	0	R/W	VGL SCP Event Interrupt Mask 0 = Not masked 1 = Masked
D[3]	DVDD_SCP_MASK	0	R/W	DVDD SCP Event Interrupt Mask 0 = Not masked 1 = Masked
D[2]	AVDD_SCP_MASK	0	R/W	AVDD SCP Event Interrupt Mask 0 = Not masked 1 = Masked
D[1]	ELVSS_SCP_MASK	0	R/W	ELVSS SCP Event Interrupt Mask 0 = Not masked 1 = Masked
D[0]	ELVDD_SCP_MASK	0	R/W	ELVDD SCP Event Interrupt Mask 0 = Not masked 1 = Masked

REGISTER MAP (continued)

REG0x08: ELVDD_SET Register Address [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3:0]	ELVDD_SET[3:0]	1000	R/W	ELVDD Output Voltage Setting: V_{ELVDD} = ELVDD_SET[3:0] × 100mV + 2.0V Offset: 2.0V Range: 2.0V (0000) ~ 3.0V (1010) Default: 2.8V (1000) If ELVDD_SET[3:0] ≥ 1010, V_{ELVDD} = 3.0V

Table 4. ELVDD Voltage Setting

Data (hex)	ELVDD (V)	Data (hex)	ELVDD (V)
0x00	2.0	0x06	2.6
0x01	2.1	0x07	2.7
0x02	2.2	0x08	2.8
0x03	2.3	0x09	2.9
0x04	2.4	0x0A	3.0
0x05	2.5	> 0x0A	3.0

REG0x09: ELVSS_SET Register Address [reset = 0x38]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	ELVSS_SET[7:0]	00111000	R/W	ELVSS Output Voltage Setting: V_{ELVSS} = - ELVSS_SET[7:0] × 50mV - 2V Range: -2.0V (00000000) ~-12.0V (11001000) Default: -4.8V (00111000) (refer to Table 5) If ELVSS_SET[7:0] ≥11001000, V_{ELVDD} = -12V

REGISTER MAP (continued)

Table 5. ELVSS Voltage Setting

Data (hex)	ELVSS (V)	Data (hex)	ELVSS (V)	Data (hex)	ELVSS (V)	Data (hex)	ELVSS (V)	Data (hex)	ELVSS (V)
0x00	-2.00	0x29	-4.05	0x52	-6.10	0x7B	-8.15	0xA4	-10.20
0x01	-2.05	0x2A	-4.10	0x53	-6.15	0x7C	-8.20	0xA5	-10.25
0x02	-2.10	0x2B	-4.15	0x54	-6.20	0x7D	-8.25	0xA6	-10.30
0x03	-2.15	0x2C	-4.20	0x55	-6.25	0x7E	-8.30	0xA7	-10.35
0x04	-2.20	0x2D	-4.25	0x56	-6.30	0x7F	-8.35	0xA8	-10.40
0x05	-2.25	0x2E	-4.30	0x57	-6.35	0x80	-8.40	0xA9	-10.45
0x06	-2.30	0x2F	-4.35	0x58	-6.40	0x81	-8.45	0xAA	-10.50
0x07	-2.35	0x30	-4.40	0x59	-6.45	0x82	-8.50	0xAB	-10.55
0x08	-2.40	0x31	-4.45	0x5A	-6.50	0x83	-8.55	0xAC	-10.60
0x09	-2.45	0x32	-4.50	0x5B	-6.55	0x84	-8.60	0xAD	-10.65
0x0A	-2.50	0x33	-4.55	0x5C	-6.60	0x85	-8.65	0xAE	-10.70
0x0B	-2.55	0x34	-4.60	0x5D	-6.65	0x86	-8.70	0xAF	-10.75
0x0C	-2.60	0x35	-4.65	0x5E	-6.70	0x87	-8.75	0xB0	-10.80
0x0D	-2.65	0x36	-4.70	0x5F	-6.75	0x88	-8.80	0xB1	-10.85
0x0E	-2.70	0x37	-4.75	0x60	-6.80	0x89	-8.85	0xB2	-10.90
0x0F	-2.75	0x38	-4.80	0x61	-6.85	0x8A	-8.90	0xB3	-10.95
0x10	-2.80	0x39	-4.85	0x62	-6.90	0x8B	-8.95	0xB4	-11.00
0x11	-2.85	0x3A	-4.90	0x63	-6.95	0x8C	-9.00	0xB5	-11.05
0x12	-2.90	0x3B	-4.95	0x64	-7.00	0x8D	-9.05	0xB6	-11.10
0x13	-2.95	0x3C	-5.00	0x65	-7.05	0x8E	-9.10	0xB7	-11.15
0x14	-3.00	0x3D	-5.05	0x66	-7.10	0x8F	-9.15	0xB8	-11.20
0x15	-3.05	0x3E	-5.10	0x67	-7.15	0x90	-9.20	0xB9	-11.25
0x16	-3.10	0x3F	-5.15	0x68	-7.20	0x91	-9.25	0xBA	-11.30
0x17	-3.15	0x40	-5.20	0x69	-7.25	0x92	-9.30	0xBB	-11.35
0x18	-3.20	0x41	-5.25	0x6A	-7.30	0x93	-9.35	0xBC	-11.40
0x19	-3.25	0x42	-5.30	0x6B	-7.35	0x94	-9.40	0xBD	-11.45
0x1A	-3.30	0x43	-5.35	0x6C	-7.40	0x95	-9.45	0xBE	-11.50
0x1B	-3.35	0x44	-5.40	0x6D	-7.45	0x96	-9.50	0xBF	-11.55
0x1C	-3.40	0x45	-5.45	0x6E	-7.50	0x97	-9.55	0xC0	-11.60
0x1D	-3.45	0x46	-5.50	0x6F	-7.55	0x98	-9.60	0xC1	-11.65
0x1E	-3.50	0x47	-5.55	0x70	-7.60	0x99	-9.65	0xC2	-11.70
0x1F	-3.55	0x48	-5.60	0x71	-7.65	0x9A	-9.70	0xC3	-11.75
0x20	-3.60	0x49	-5.65	0x72	-7.70	0x9B	-9.75	0xC4	-11.80
0x21	-3.65	0x4A	-5.70	0x73	-7.75	0x9C	-9.80	0xC5	-11.85
0x22	-3.70	0x4B	-5.75	0x74	-7.80	0x9D	-9.85	0xC6	-11.90
0x23	-3.75	0x4C	-5.80	0x75	-7.85	0x9E	-9.90	0xC7	-11.95
0x24	-3.80	0x4D	-5.85	0x76	-7.90	0x9F	-9.95	0xC8	-12.00
0x25	-3.85	0x4E	-5.90	0x77	-7.95	0xA0	-10.00	> 0xC8	-12.00
0x26	-3.90	0x4F	-5.95	0x78	-8.00	0xA1	-10.05		
0x27	-3.95	0x50	-6.00	0x79	-8.05	0xA2	-10.10		
0x28	-4.00	0x51	-6.05	0x7A	-8.10	0xA3	-10.15		

REGISTER MAP (continued)

REG0x0A: AVDD_SET Register Address [reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4:0]	AVDD_SET[4:0]	01010	R/W	AVDD Output Voltage Setting: V_{AVDD} = AVDD_SET[4:0] × 100mV + 5.5V Range: 5.5V (00000) ~ 7.9V (11000) Default: 6.5V (01010) If AVDD_SET[4:0] ≥ 11000, V_{AVDD} = 7.9V

Table 6. AVDD Voltage Setting

Data (hex)	AVDD (V)	Data (hex)	AVDD (V)	Data (hex)	AVDD (V)
0x00	5.5	0x09	6.4	0x12	7.3
0x01	5.6	0x0A	6.5	0x13	7.4
0x02	5.7	0x0B	6.6	0x14	7.5
0x03	5.8	0x0C	6.7	0x15	7.6
0x04	5.9	0x0D	6.8	0x16	7.7
0x05	6.0	0x0E	6.9	0x17	7.8
0x06	6.1	0x0F	7.0	0x18	7.9
0x07	6.2	0x10	7.1	> 0x18	7.9
0x08	6.3	0x11	7.2		

REGISTER MAP (continued)

REG0x0B: DVDD_SET Register Address [reset = 0x14, 0x28 or 0x32]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	DVDD_SET[6:0]	0010100 or 0101000 or 0110010	R/W	DVDD Output Voltage Setting: V_{DVDD} = DVDD_SET[6:0] × 10mV + 0.8V Range: 0.8V (0000000) ~ 1.5V (1000110) Default: 1.0V (0010100), 1.2V (0101000) or 1.3V (0110010) If DVDD_SET[6:0] ≥1000110, V_{DVDD} = 1.5V The default DVDD voltage is decided by DVDD_SEL: DVDD_SEL = high, DVDD_SET[6:0] = 0010100 (1.0V) DVDD_SEL = low, DVDD_SET[6:0] = 0101000 (1.2V) DVDD_SEL = Floating, DVDD_SET[6:0] = 0110010 (1.3V)

Table 7. DVDD Voltage Setting

Data (hex)	DVDD (V)	Data (hex)	DVDD (V)	Data (hex)	DVDD (V)	Data (hex)	DVDD (V)	Data (hex)	DVDD (V)
0x00	0.80	0x10	0.96	0x20	1.12	0x30	1.28	0x40	1.44
0x01	0.81	0x11	0.97	0x21	1.13	0x31	1.29	0x41	1.45
0x02	0.82	0x12	0.98	0x22	1.14	0x32	1.30	0x42	1.46
0x03	0.83	0x13	0.99	0x23	1.15	0x33	1.31	0x43	1.47
0x04	0.84	0x14	1.00	0x24	1.16	0x34	1.32	0x44	1.48
0x05	0.85	0x15	1.01	0x25	1.17	0x35	1.33	0x45	1.49
0x06	0.86	0x16	1.02	0x26	1.18	0x36	1.34	0x46	1.50
0x07	0.87	0x17	1.03	0x27	1.19	0x37	1.35	> 0x46	1.50
0x08	0.88	0x18	1.04	0x28	1.20	0x38	1.36		
0x09	0.89	0x19	1.05	0x29	1.21	0x39	1.37		
0x0A	0.90	0x1A	1	0x2A	1.22	0x3A	1.38		
0x0B	0.91	0x1B	1.07	0x2B	1.23	0x3B	1.39		
0x0C	0.92	0x1C	1.08	0x2C	1.24	0x3C	1.40		
0x0D	0.93	0x1D	1.09	0x2D	1.25	0x3D	1.41		
0x0E	0.94	0x1E	1.10	0x2E	1.26	0x3E	1.42		
0x0F	0.95	0x1F	1.11	0x2F	1.27	0x3F	1.43		

REGISTER MAP (continued)

REG0x0C: VGL_SET Register Address [reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	VGL_SET[6:0]	0111100	R/W	VGL Output Voltage Setting: V_{VGL} = - VGL_SET[6:0] × 100mV - 5V Range: -5V (0000000) ~ -15V (1100100) Default: -11V (0111100) If VGL_SET[6:0] ≥1100100, V_{GL} = -15V

Table 8. VGL Voltage Setting

Data (hex)	VGL (V)	Data (hex)	VGL (V)	Data (hex)	VGL (V)	Data (hex)	VGL (V)	Data (hex)	VGL (V)
0x00	-5.0	0x15	-7.1	0x2A	-9.2	0x3F	-11.3	0x54	-13.4
0x01	-5.1	0x16	-7.2	0x2B	-9.3	0x40	-11.4	0x55	-13.5
0x02	-5.2	0x17	-7.3	0x2C	-9.4	0x41	-11.5	0x56	-13.6
0x03	-5.3	0x18	-7.4	0x2D	-9.5	0x42	-11.6	0x57	-13.7
0x04	-5.4	0x19	-7.5	0x2E	-9.6	0x43	-11.7	0x58	-13.8
0x05	-5.5	0x1A	-7.6	0x2F	-9.7	0x44	-11.8	0x59	-13.9
0x06	-5.6	0x1B	-7.7	0x30	-9.8	0x45	-11.9	0x5A	-14.0
0x07	-5.7	0x1C	-7.8	0x31	-9.9	0x46	-12.0	0x5B	-14.1
0x08	-5.8	0x1D	-7.9	0x32	-10.0	0x47	-12.1	0x5C	-14.2
0x09	-5.9	0x1E	-8.0	0x33	-10.1	0x48	-12.2	0x5D	-14.3
0x0A	-6.0	0x1F	-8.1	0x34	-10.2	0x49	-12.3	0x5E	-14.4
0x0B	-6.1	0x20	-8.2	0x35	-10.3	0x4A	-12.4	0x5F	-14.5
0x0C	-6.2	0x21	-8.3	0x36	-10.4	0x4B	-12.5	0x60	-14.6
0x0D	-6.3	0x22	-8.4	0x37	-10.5	0x4C	-12.6	0x61	-14.7
0x0E	-6.4	0x23	-8.5	0x38	-10.6	0x4D	-12.7	0x62	-14.8
0x0F	-6.5	0x24	-8.6	0x39	-10.7	0x4E	-12.8	0x63	-14.9
0x10	-6.6	0x25	-8.7	0x3A	-10.8	0x4F	-12.9	0x64	-15.0
0x11	-6.7	0x26	-8.8	0x3B	-10.9	0x50	-13.0	> 0x64	-15.0
0x12	-6.8	0x27	-8.9	0x3C	-11.0	0x51	-13.1		
0x13	-6.9	0x28	-9.0	0x3D	-11.1	0x52	-13.2		
0x14	-7.0	0x29	-9.1	0x3E	-11.2	0x53	-13.3		

REGISTER MAP (continued)

REG0x0D: DEVICE_INFO Register Address [reset = 0x52]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	PRODUCT_ID[3:0]	0101	R	Manufacture ID
D[3:0]	DEVICE_ID[3:0]	0010	R	Device ID

REG0x0E: ELVSS_FREQ_SET Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4:3]	ELVSS_FREQ_SET	00	R/W	ELVSS Operation Frequency Control at light load of auto-mode: 00 = No Setting (default) 01 = Frequency > 200Hz 10 = Frequency > 2.5kHz 11 = Frequency > 5kHz
D[2:0]	Reserved	000	R/W	Reserved

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2023 – REV.A.1 to REV.A.2 **Page**

Deleted Detailed Description section 23
Deleted Register Map section 34

NOVEMBER 2023 – REV.A to REV.A.1 **Page**

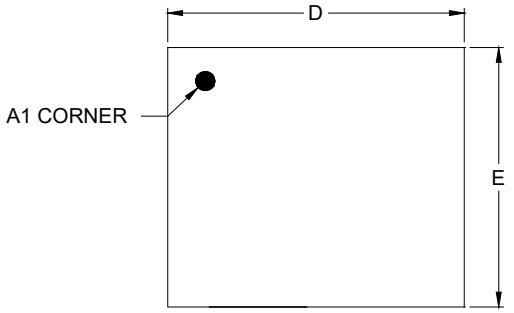
Changed Features section 1
Added Absolute Maximum Ratings section 2
Added Electrical Characteristics section 6
Deleted Figure 5 22
Changed Register Map section 40

Changes from Original (OCTOBER 2023) to REV.A **Page**

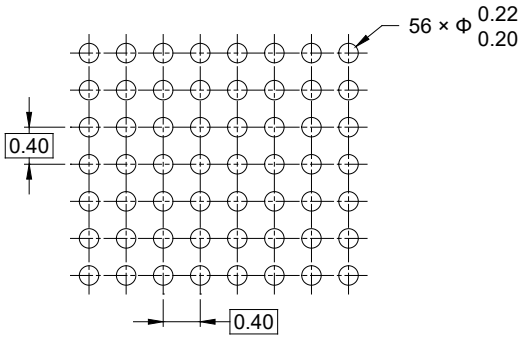
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

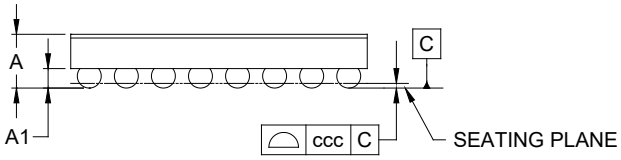
WLCSP-3.2×2.8-56B



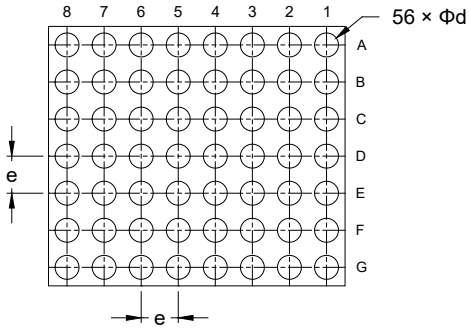
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



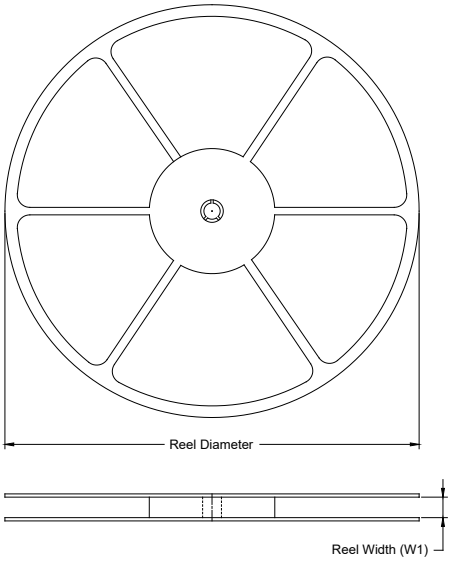
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.625
A1	0.190	-	0.230
D	3.170	-	3.230
E	2.770	-	2.830
d	0.228	-	0.288
e	0.400 BSC		
ccc	0.050		

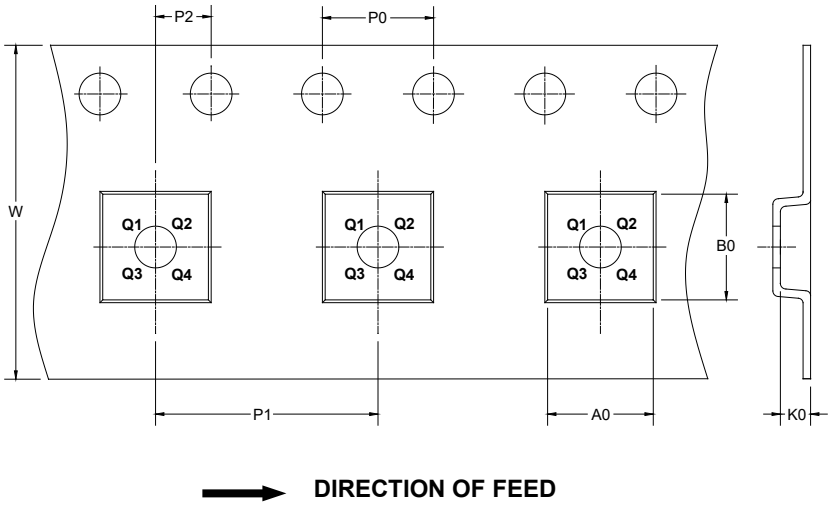
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



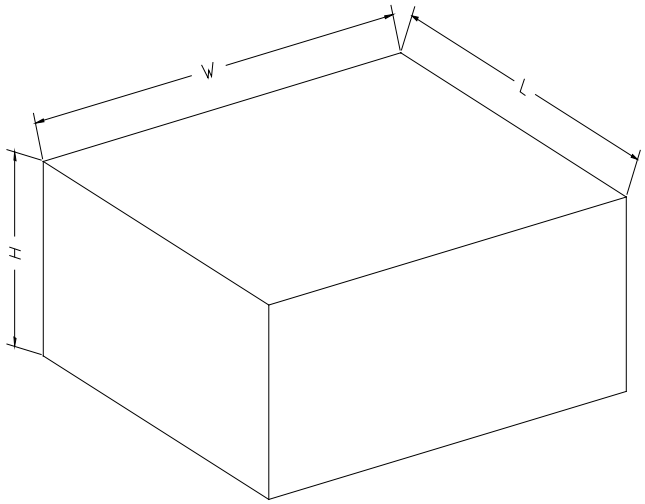
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.2×2.8-56B	7"	12.4	3.03	3.42	0.73	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002