SGM4590
GOA Panel 15-Channel Level Shifter

GENERAL DESCRIPTION

The SGM4590 is a 15-channel high-voltage level shifter for GOA TFT-LCD panel application. It features adjustable gate pattern function.

The SGM4590 is used for transferring the logic signals that are generated by the TCON system. Different outputs of CKO_1~CKO_8 will be generated by the different settings which are outside the device. The low-impedance transistors that are located at the outputs of the device will generate fast transit, even driving the LCD panel (a capacitive load).

The SGM4590 has the input under-voltage lockout (UVLO) and the over-temperature protection (OTP) functions.

The SGM4590 is available in a Green TQFN-4×4-32L package and it operates over the temperature range of -40℃ to +85℃.

FEATURES

- **15-Channel Level Shifter**
- **Input Supply Range: 2.5V to 5.5V**
- **Input Under-Voltage Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
- **Highest Voltage Level: +30V**
- **Lowest Voltage Level: -10V**
- **Peak Current: 800mA**
- **Continuous Current: 30mA**
- **Available in a Green TQFN-4×4-32L Package**

APPLICATIONS

GOA TFT-LCD Panel

TYPICAL APPLICATION

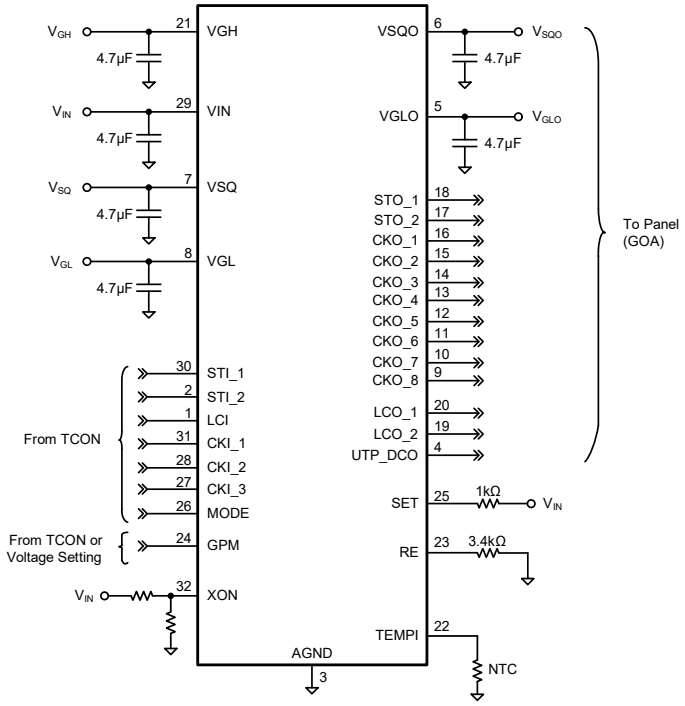


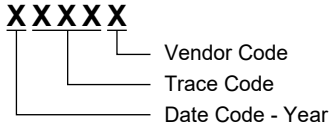
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4590	TQFN-4×4-32L	-40℃ to +85℃	SGM4590YTQU32G/TR	SGM4590 YTQU32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to AGND)
VIN ..... -0.3V to 6V
STI_1, STI_2, LCI, CKI_1~CKI_3 .....-0.3V to V_{IN} + 0.3V
SET, MODE, GPM, TEMPI, XON .....-0.3V to V_{IN} + 0.3V
VGH ..... -0.3V to 40V
VGL, VSQ ..... -20V to 0.3V
RE ..... -0.3V to V_{GH} + 0.3V
LCO_1, LCO_2, UTP_DCO, VSQO to VSQ
..... -0.3V to V_{GH} + 0.3V
CKO_1~CKO_8, STO_1, STO_2, VGLO to VGL
..... -0.3V to V_{GH} + 0.3V
VGH to VGL, VSQ ..... -0.3V to 50V
Package Thermal Resistance
TQFN-4×4-32L, θ_{JA} ..... 38℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM 8000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .....-40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

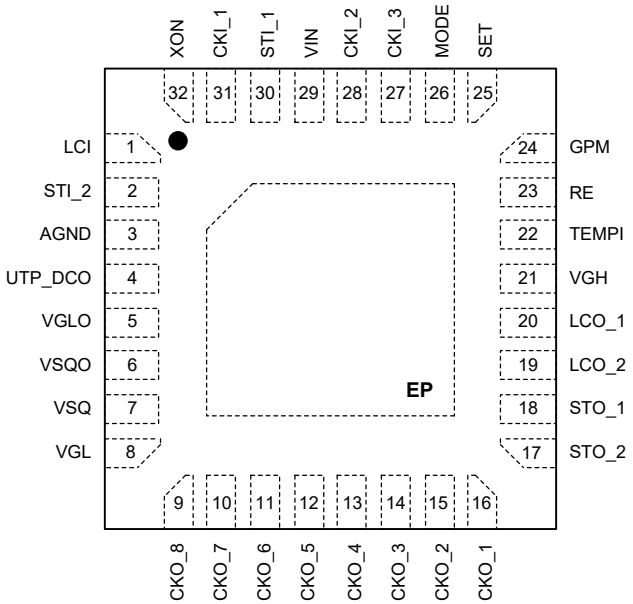
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-32L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	LCI	Input Signal for Level Shifter (Low Frequency Clock). The LCI is the high-/low-level trigger.
2	STI_2	Input Signal for Level Shifter (Start Pulse when MODE = High-Level and Stop Pulse when MODE = Low-Level). The STO_2 is the output of the specific level shifter.
3	AGND	Analog Ground for Logic Block.
4	UTP_DCO	Output Signal. Default output is VSQ, output VGH when TEMPI = High.
5	VGLO	Output Signal, Discharge Function for Liquid Crystal Capacitor. Low output = VGL.
6	VSQO	Output Signal, Discharge Function for Liquid Crystal Capacitor. Low output = VSQ.
7	VSQ	Negative Power Supply (LCO_1, LCO_2 and UTP_DCO).
8	VGL	Negative Power Supply (CKO_1~CKO_8, STO_1 and STO_2).
9, 10, 11, 12, 13, 14, 15, 16	CKO_8~CKO_1	Output Signal for Level Shifter.
17, 18	STO_2, STO_1	Output Signal for Level Shifter.
19	LCO_2	Output Signal for Level Shifter (Low Frequency Clock 2).
20	LCO_1	Output Signal for Level Shifter (Low Frequency Clock 1).
21	VGH	Positive Power Supply (STO_1, STO_2, LCO_1, LCO_2, CKO_1~CKO_8 and UTP_DCO).
22	TEMPI	Input Signal for UTP Function.
23	RE	Resistor Connection Input for GPM Function.
24	GPM	Setting Pin for GPM Function. High-level: shave falling edge.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
25	SET	Phase Selection Setting Pin. VIN: 8 phase. AGND: 6 phase. Floating: 4 phase. Change the setting at every START rising edge.
26	MODE	CKO_x Output Sequence Selection Setting Pin. High-level: CKO_8 output first. Low-level: CKO_1 output first. Change the setting at every STOP falling edge.
27	CKI_3	Input Signal for GPM Function.
28	CKI_2	Input Signal (Duty Cycle Adjust). The CKI_2 is the high-/low-level trigger.
29	VIN	Supply Voltage Input.
30	STI_1	Input Signal for Level Shifter (Start Pulse when MODE = Low-Level and Stop Pulse when MODE = High-Level). The STO_1 is the output of the specific level shifter.
31	CKI_1	Input Signal for Level Shifter (Condensed Clock). The CKI_1 is the high-/low-level trigger.
32	XON	Input Signal for XON Function.
Exposed Pad	EP	Thermal Pad. No connection.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, T_A = +25℃, V_{GH} = 22V, V_{GL} = V_{SQ} = -7V and AGND = 0V, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General							
Supply Voltage		V_{IN}	Operating	2.5		5.5	V
VIN Under-Voltage Lockout Threshold		V_{IN_UVLO}	VIN rising, hysteresis 200mV	1.75	1.95	2.05	V
XON Voltage External Setting		V_{XON}	VIN falling, reference voltage, V_{IN} = 2.5V to 5.5V	0.42		0.56	V
VGH Under-Voltage Lockout Threshold		V_{GH_UVLO}	VGH rising	6.1		7	V
			VGH falling	3		3.8	
UTP Function		V_{REF}	V_{IN} = 2.5V to 5.5V, see Figure 8	0.95		1.35	V
		V_{TEMPI}	COMP threshold voltage, V_{IN} = 2.5V to 5.5V, see Figure 8	0.35		0.55	V
		R_1	See Figure 8	55		125	kΩ
Thermal Overload Shutdown		t_{SD}	Junction temperature rising		165		℃
Level Shifter							
VGH to AGND				7		30	V
VGL, VSQ to AGND				-10		0	V
VGH - (VGL or VSQ)						40	V
LCO_1, LCO_2, VSQO, UTP_DCO		V_{OUT}		V_{SQ} + 0.1		V_{GH} - 0.2	V
CKO_1~CKO_8, STO_1, STO_2, VGLO				V_{GL} + 0.1		V_{GH} - 0.1	V
Input High-Level (CKI_1~CKI_3, GPM, STI_1, STI_2, LCI)		V_{IH}	V_{IN} = 2.5V to 5.5V	1.4			V
Input Low-Level (CKI_1~CKI_3, GPM, STI_1, STI_2, LCI)		V_{IL}	V_{IN} = 2.5V to 5.5V			0.5	V
Positive Output Swing	CKO_1~CKO_8, STO_1, STO_2, LCO_1, LCO_2, VSQO, VGLO, UTP_DCO	V_{CK+}	All inputs high, I_O = 10mA	V_{GH} - 0.3	V_{GH} - 0.1	V_{GH}	V
Negative Output Swing	LCO_1, LCO_2, UTP_DCO, VSQO	V_{CK-}	All inputs low, I_O = -10mA	V_{SQ}	V_{SQ} + 0.1	V_{SQ} + 0.3	V
	CKO_1~CKO_8, STO_1, STO_2, VGLO			V_{GL}	V_{GL} + 0.1	V_{GL} + 0.3	
High-side Switch-On Resistance	VSQO, VGLO, UTP_DCO	$R_{HIGH-SIDE}$	I_O = 10mA	10	14	18	Ω
	STO_1, STO_2			7	10	13	
	LCO_1, LCO_2			4.5	6.8	9	
	CKO_1~CKO_8			4	6.5	8.5	
Low-side Switch-On Resistance	CKO_1~CKO_8	$R_{LOW-SIDE}$	I_O = -10mA	1	3	5	Ω
	STO_1, STO_2			3.5	5.6	8	
	LCO_1, LCO_2			3	4.7	7	
	VSQO, VGLO, UTP_DCO			5	7	10	
CKO_1~CKO_8 to RE Switch On-Resistance		R_{RE}		100	140	180	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_A = +25℃, V_{GH} = 22V, V_{GL} = V_{SQ} = -7V and AGND = 0V, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Level Shifter							
Rising Time	CKO_1~CKO_8	t_R	C_L = 4.7nF, 10% ~ 90%		206	350	ns
	STO_1, STO_2				284	450	
	LCO_1, LCO_2				215	450	
Falling Time	CKO_1~CKO_8	t_F	C_L = 4.7nF, 90% ~ 10%		171	400	ns
	STO_1, STO_2				309	550	
	LCO_1, LCO_2				237	550	
Rising Edge Delay Time	CKO_1~CKO_8	t_{RD}	C_L = 4.7nF, 50% of input to 10% of output		151	200	ns
	STO_1, STO_2				146	200	
	LCO_1, LCO_2				164	200	
Falling Edge Delay Time	CKO_1~CKO_8	t_{FD}	C_L = 4.7nF, 50% of input to 90% of output		388	450	ns
	STO_1, STO_2				394	450	
	LCO_1, LCO_2				360	450	

FUNCTIONAL BLOCK DIAGRAM

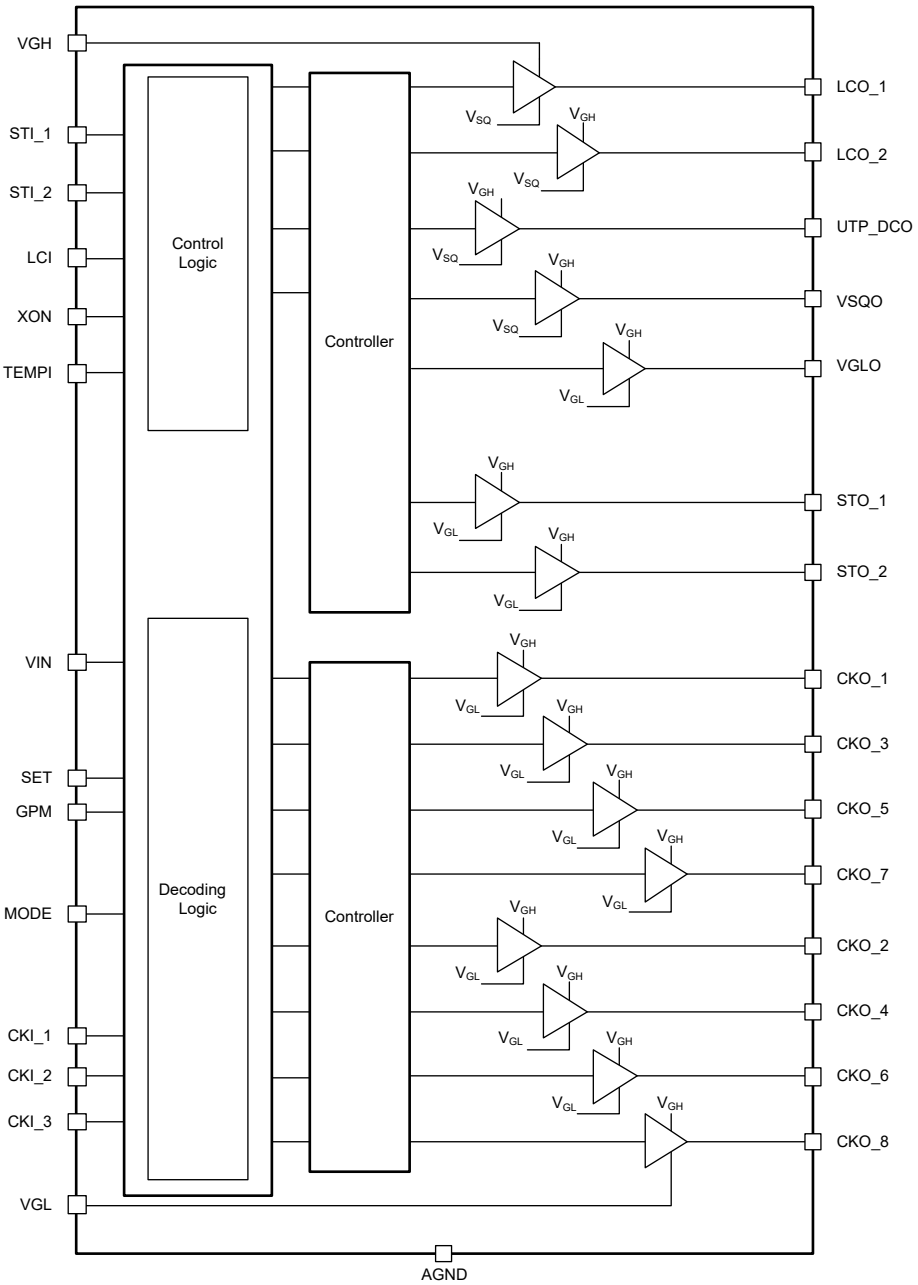


Figure 2. Block Diagram

DETAILED DESCRIPTION

Power-On Sequence

The internal signal ENA for condensed GOA logic goes high if the V_{IN} exceeds V_{IN_UVLO}. The level shifter outputs CKO_1~CKO_8, STO_1 and STO_2 track the VGL supply, and LCO_1 and LCO_2 track the VSQ supply, which is called default mode. After V_{GH} exceeds V_{GH_UVLO}, the default mode continues until receiving the first START rising edge. Input signals STI_1 and STI_2 will provide START and STOP commands. LCO_1 and LCO_2 only refresh in the period after STOP and before the next START. Refer to Figure 3.

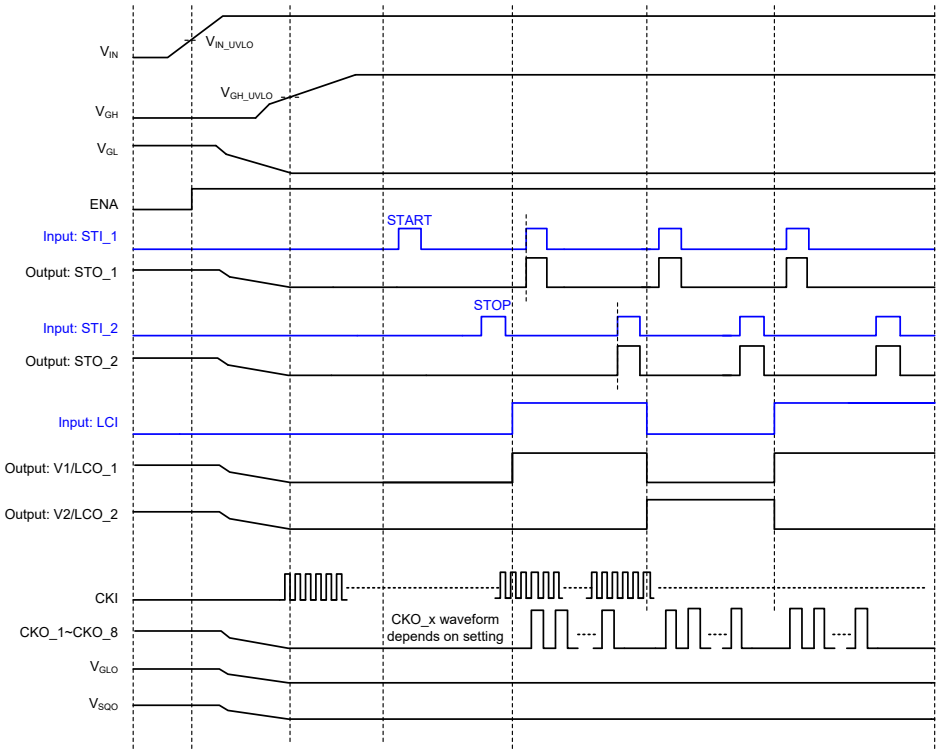


Figure 3. Power-On Waveform Diagram

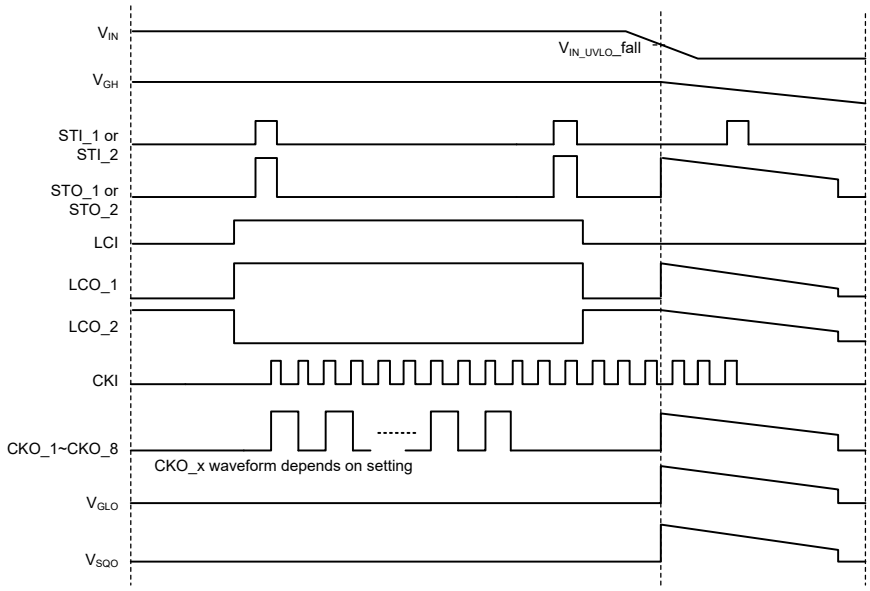


Figure 4. Power-Off Waveform Diagram

DETAILED DESCRIPTION (continued)

Power-Off Sequence (XON Mode)

The falling V_{IN_UVLO} reference voltage at the XON pin is 0.5V. The user selects a resistor divider to obtain the falling threshold for the specific application. The thresholds can be determined as follows:

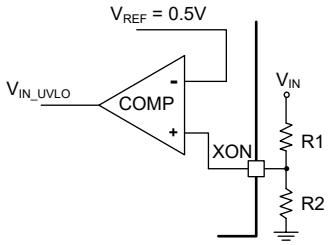


Figure 5. XON Function Structure

Once the level of V_{IN} is below the V_{REF}, the output of the SGM4590 will be pulled at the same level as VGH. Refer to Figure 4.

Level Shift Function

The SGM4590 contains 15-channel level shifter. The corresponding tech is Gate-On-Array (GOA). Four signals are used to generate signals of STO_1, STO_2, LCO_1, LCO_2, and CKO_1~CKO_8. VGL is the low-level for CKO_1~CKO_8, STO_1 and STO_2 while VSQ is the low-level for LCO_1 and LCO_2. The settings for the output of the SGM4590 are shown below.

LC

The complementary signal and the two low frequency components should be taken into consideration. As a result, the LCI should be followed by LCO_1 and the inverting of the LCO_1 should be followed by LCO_2.

SET

The phase number of the CKO_x is set by the SET pin of the SGM4590. For the rising edge of each START condition, the SET will be latched and triggered. However, if there is noise interference, the state real time will be changed. Table 1 lists the settings.

Table 1. The Setting Table

Pin	Status	Level Shifter Output
SET (1)	VIN	8 phases. CKO_1~CKO_8 output.
	AGND	6 phases. CKO_1~CKO_6 output. CKO_7 and CKO_8 keep in VGL.
	Floating	4 phases. CKO_1~CKO_4 output. CKO_5~CKO_8 keep in VGL.
MODE	Logic signal high	CKO_8 output first.
	Logic signal low	CKO_1 output first.
GPM	Logic signal high	CKO_x' falling edge shaved.
	Logic signal low	Falling edge shave function disable.

NOTE: 1. For a tri-state setting pin, it is connected 400kΩ resistor to VIN and 400kΩ to AGND inside the SGM4590.

MODE

MODE pin is to set the CKO_x output sequence. CKO_1 outputs first when MODE pin = "Low". When MODE pin = "High", CKO_8 outputs first. The first type of the output for CKO_1 is shown as below (see Figure 6).

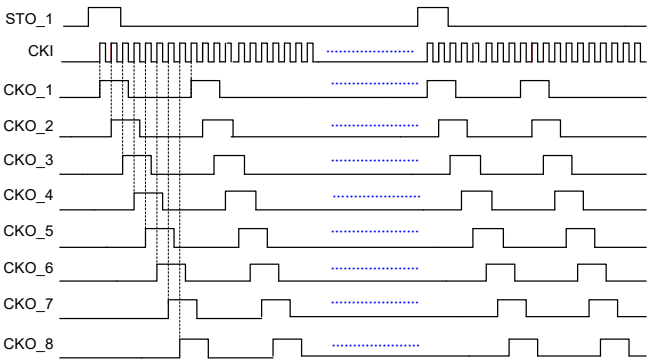


Figure 6. CKO_1 Output First Type

The first type of the output for CKO_8 is shown in Figure 7.

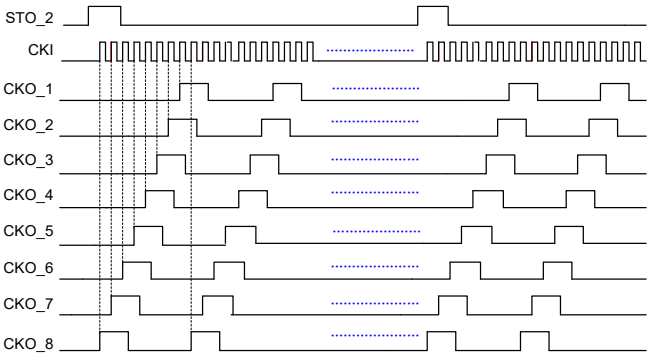


Figure 7. CKO_8 Output First Type

DETAILED DESCRIPTION (continued)

OTP

The over-temperature protection will cause the external power dissipation to the SGM4590 since the device is overheated. If the junction temperature is over 165℃, the thermal sensor that is at the internal of the SGM4590 will be triggered so that the OTP is launched. Only cycle the VIN to clear the OTP latch and reactivate the device.

UTP

The SGM4590 has an external UTP (Under-Temperature Protection) function through the input TEMPI pin. TEMPI pin supports both high-/low-level trigger and NTC mode.

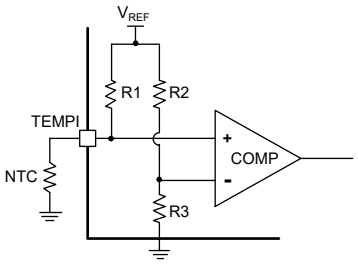


Figure 8. UTP Function Structure

CKO_x Duty Cycle Adjustable

The CKO_x output duty cycle can be adjusted through CKI_2. The first CKO_x output rising edge follows CKI_2.

GPM Function

The eight clock channels of CKO_1~CKO_8 outputs support the GPM function, which shaves the corner of the scan-driver outputs' falling edge. Depending on GPM pin, the corner of the falling edge shaving is achieved by turning off the scan-driver switches, and turn on the GPM switches to let the panel load capacitance discharge through the resistor at the RE pin. The start point of shaving activity is adjusted by CKI_3.

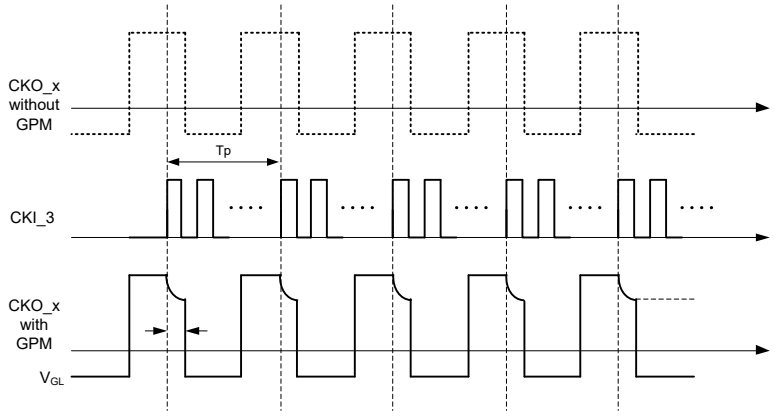


Figure 9. GPM Function Timing Sequence

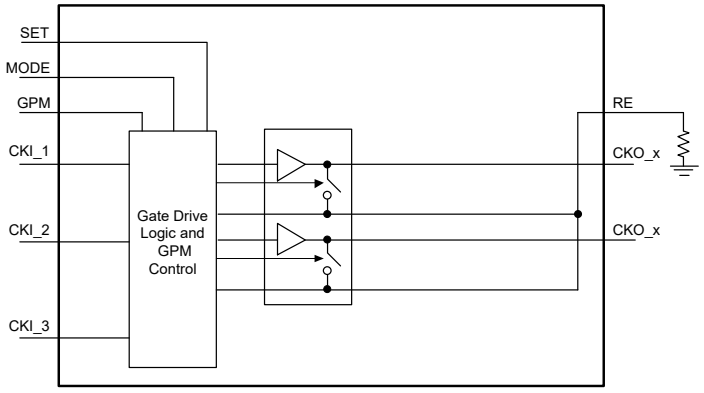


Figure 10. GPM Function Structure

DETAILED DESCRIPTION (continued)

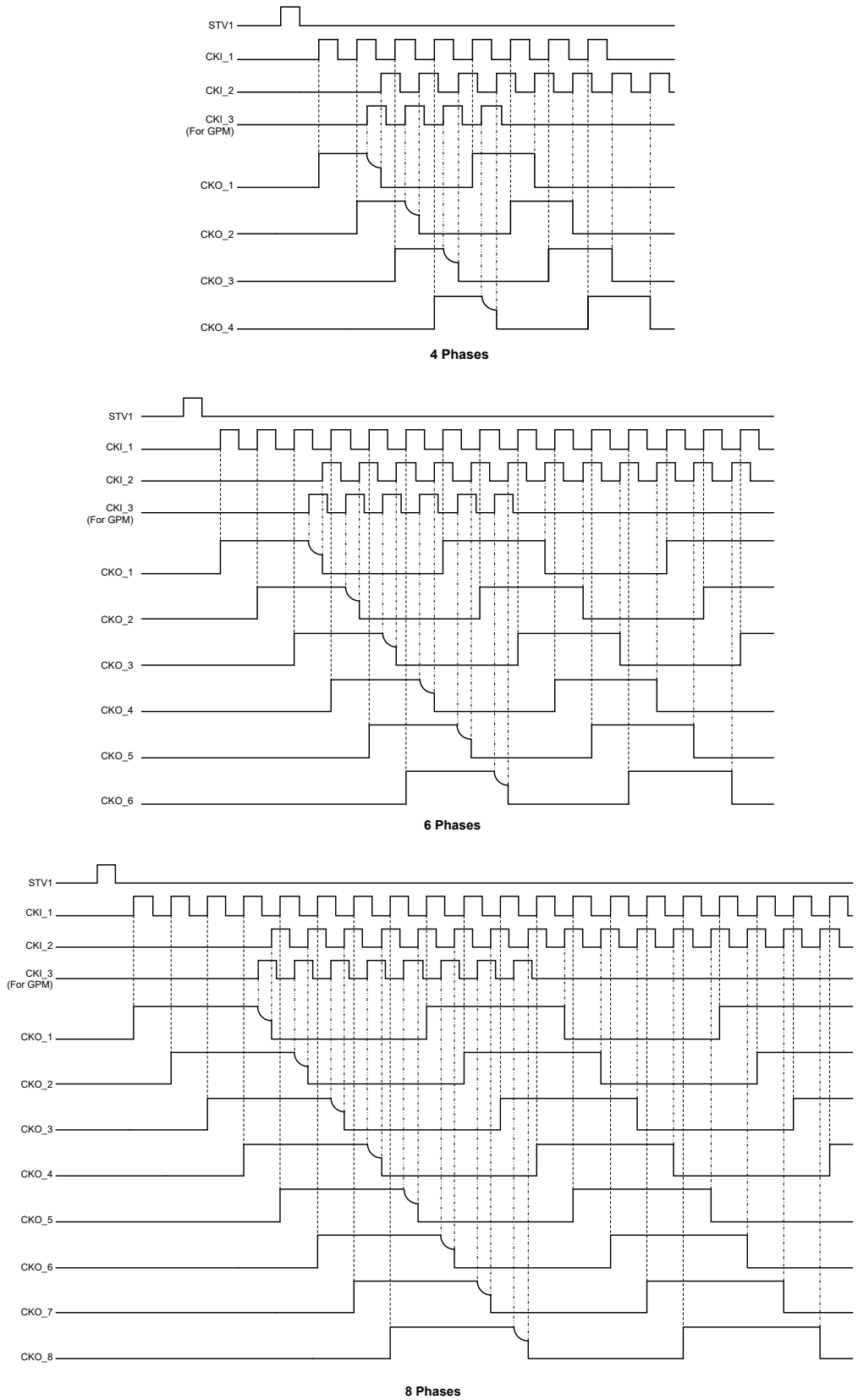


Figure 11. Timing Sequence of CKO_x

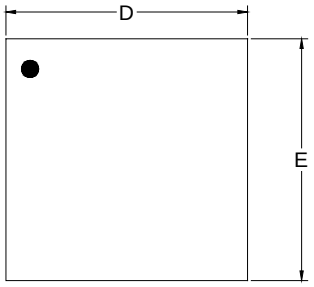
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

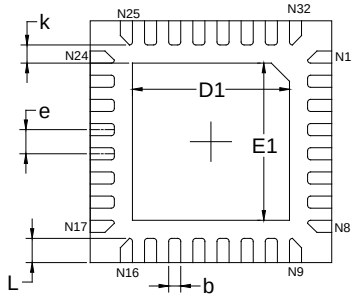
Changes from Original (MARCH 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

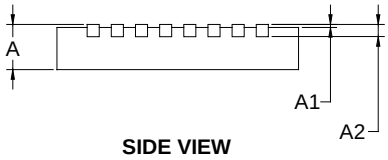
TQFN-4×4-32L



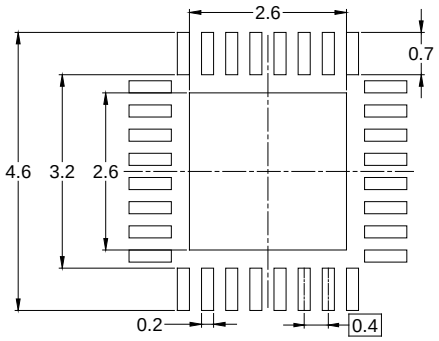
TOP VIEW



BOTTOM VIEW



SIDE VIEW



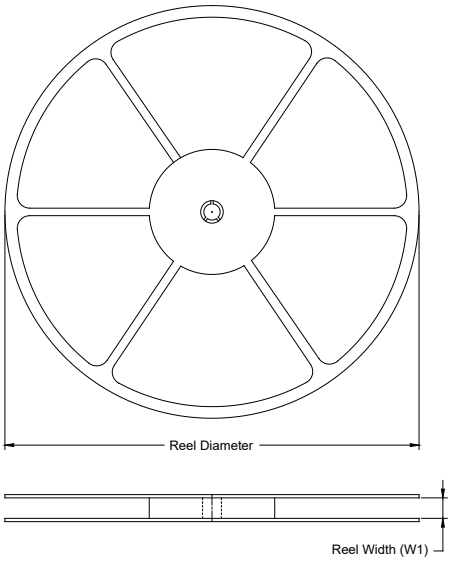
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.500	2.700	0.098	0.106
E	3.900	4.100	0.154	0.161
E1	2.500	2.700	0.098	0.106
k	0.300 REF		0.012 REF	
b	0.150	0.250	0.006	0.010
L	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	

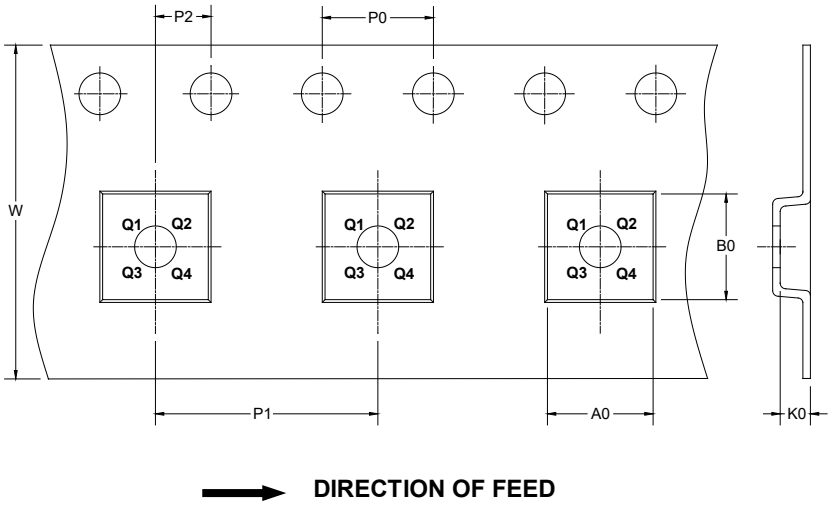
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

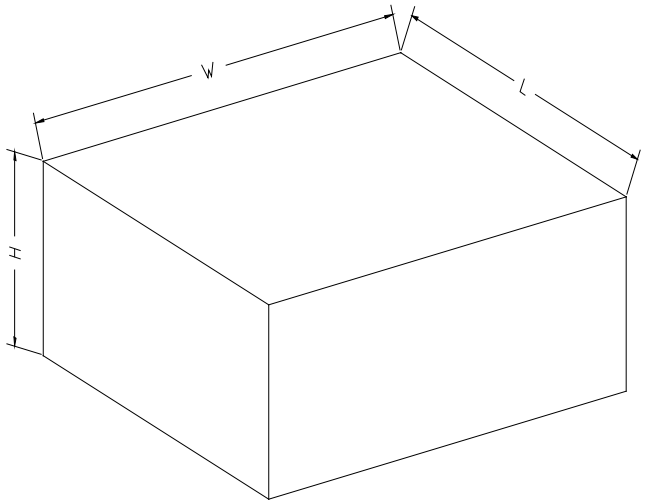
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-32L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002